ETH zürich

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

End-to-end open-source IC design

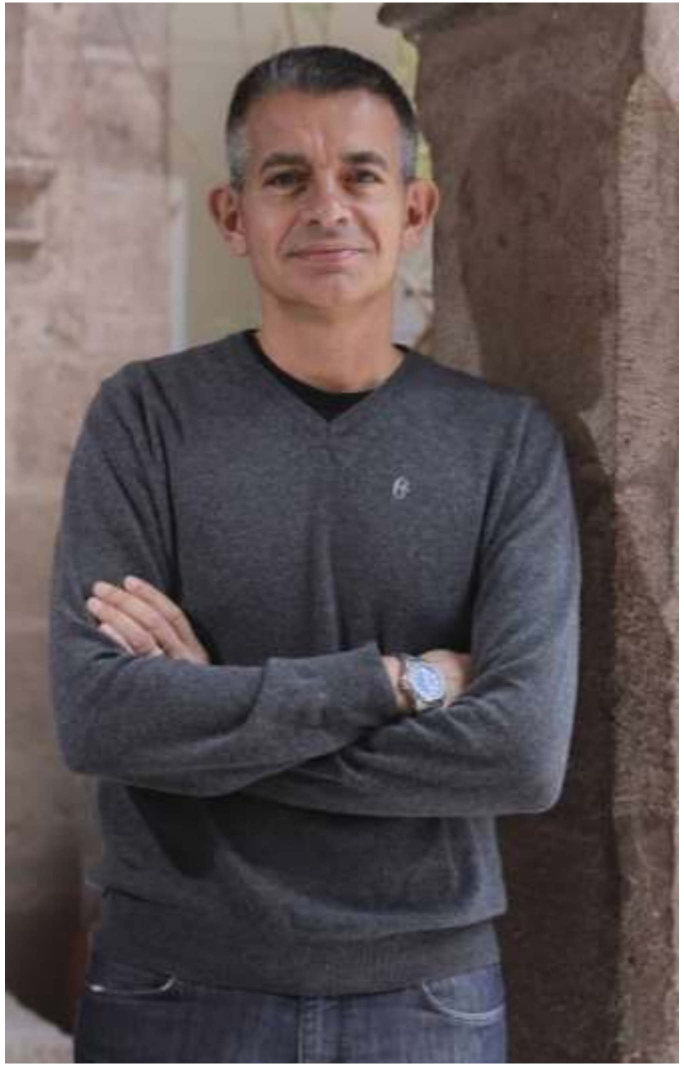
Digital Circuits and Systems Group and the PULP team

Frank K. Gürkaynak kgf@iis.ee.ethz.ch

PULP Platform
Open Source Hardware, the way it should be!

pulp-platform.org
@pulp_platform
company/pulp-platform
youtube.com/pulp_platform

PULP team at ETH Zürich: Open-source HW since 2013



- **Led by Luca Benini**
  - Professor at ETH Zürich and University of Bologna
- **Large team of around 100 people**

- **Parallel Ultra Low Power (PULP) platform**
  - https://pulp-platform.org/
  - https://x.com/pulp_platform

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2025 VLSI SYMPOSIUM

We have designed over 60 ASICs using open-source HW

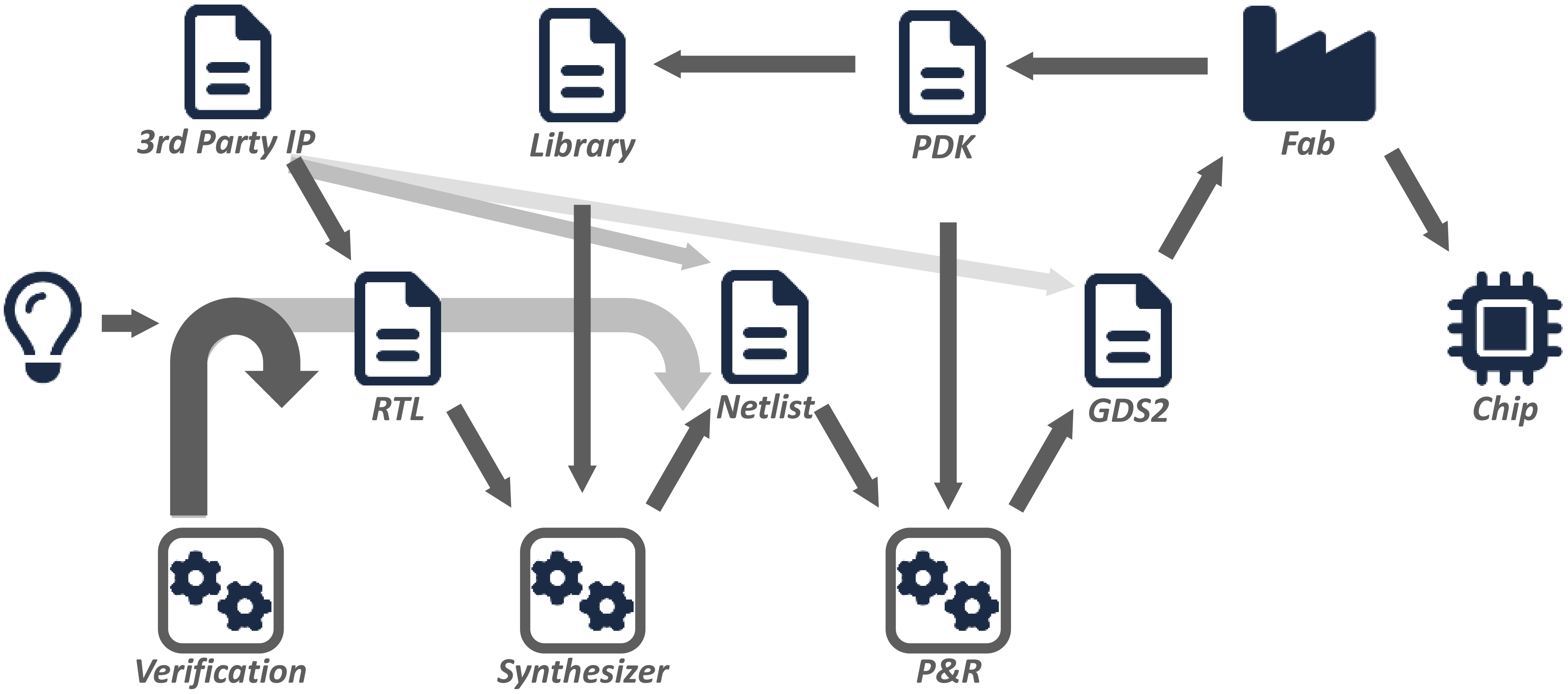
All our designs are based on open-source HW published on our GitHub page

- All using a permissive open source license (SolderPad)

`https://github.com/pulp-platform`

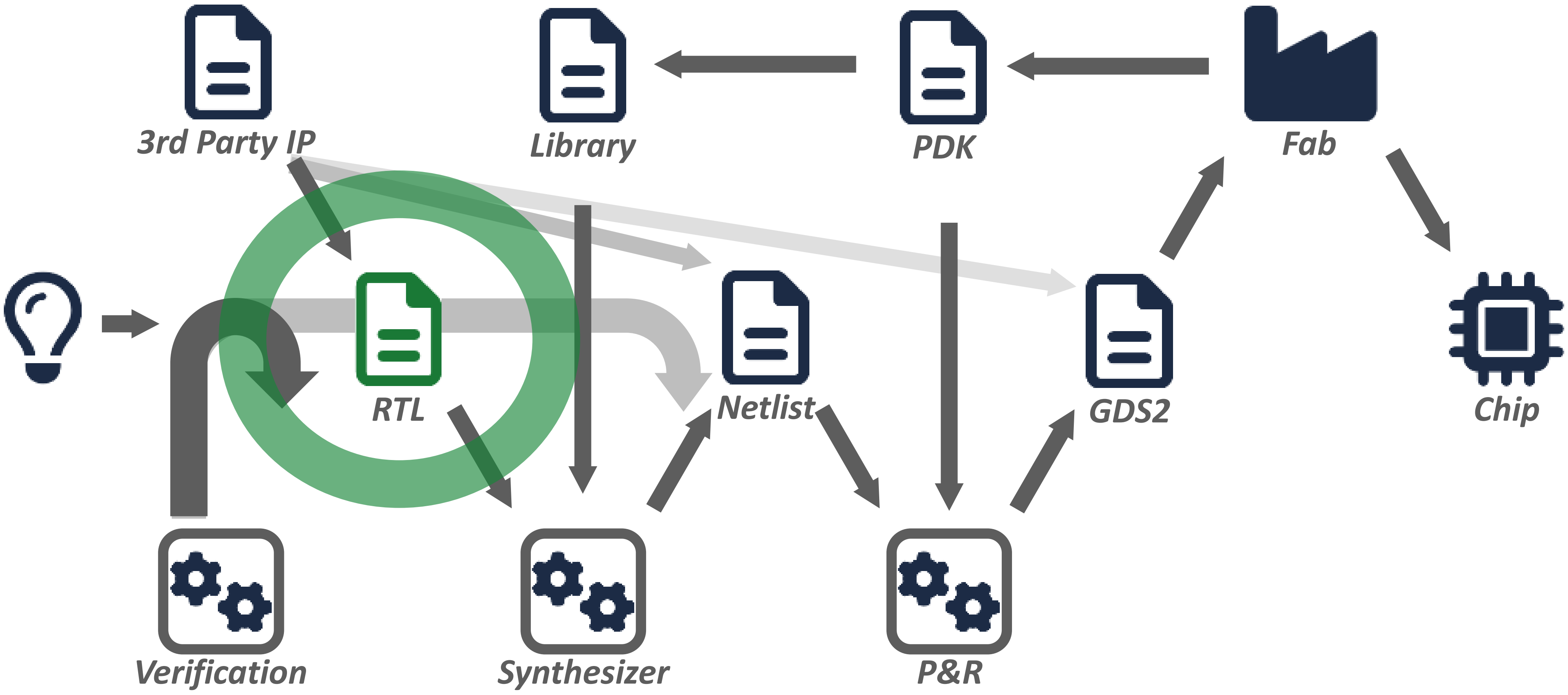
See our chip gallery under: `http://asic.ethz.ch/`

Simplified IC design flow



Icons taken from free icons from fontawesome.com

Simplified IC design flow: at the moment only RTL



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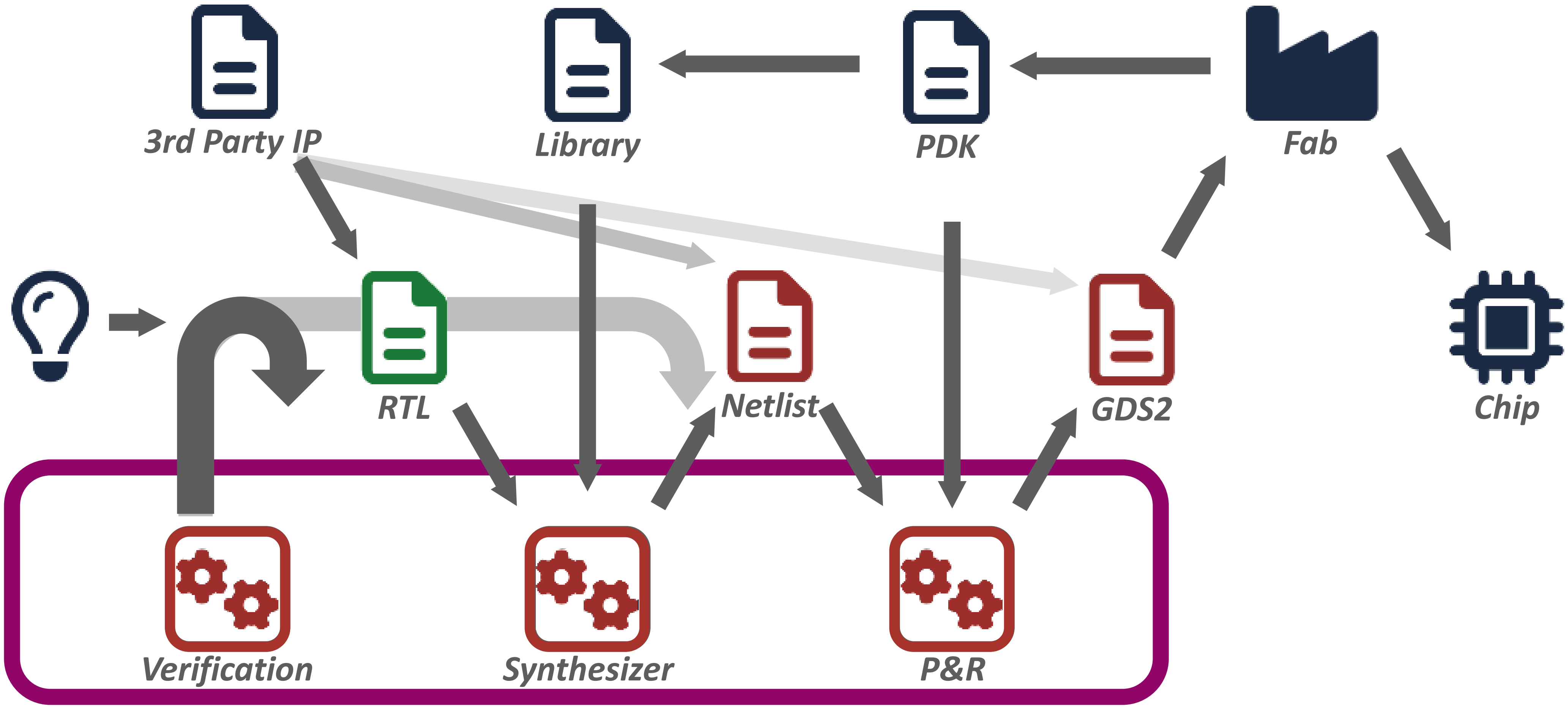
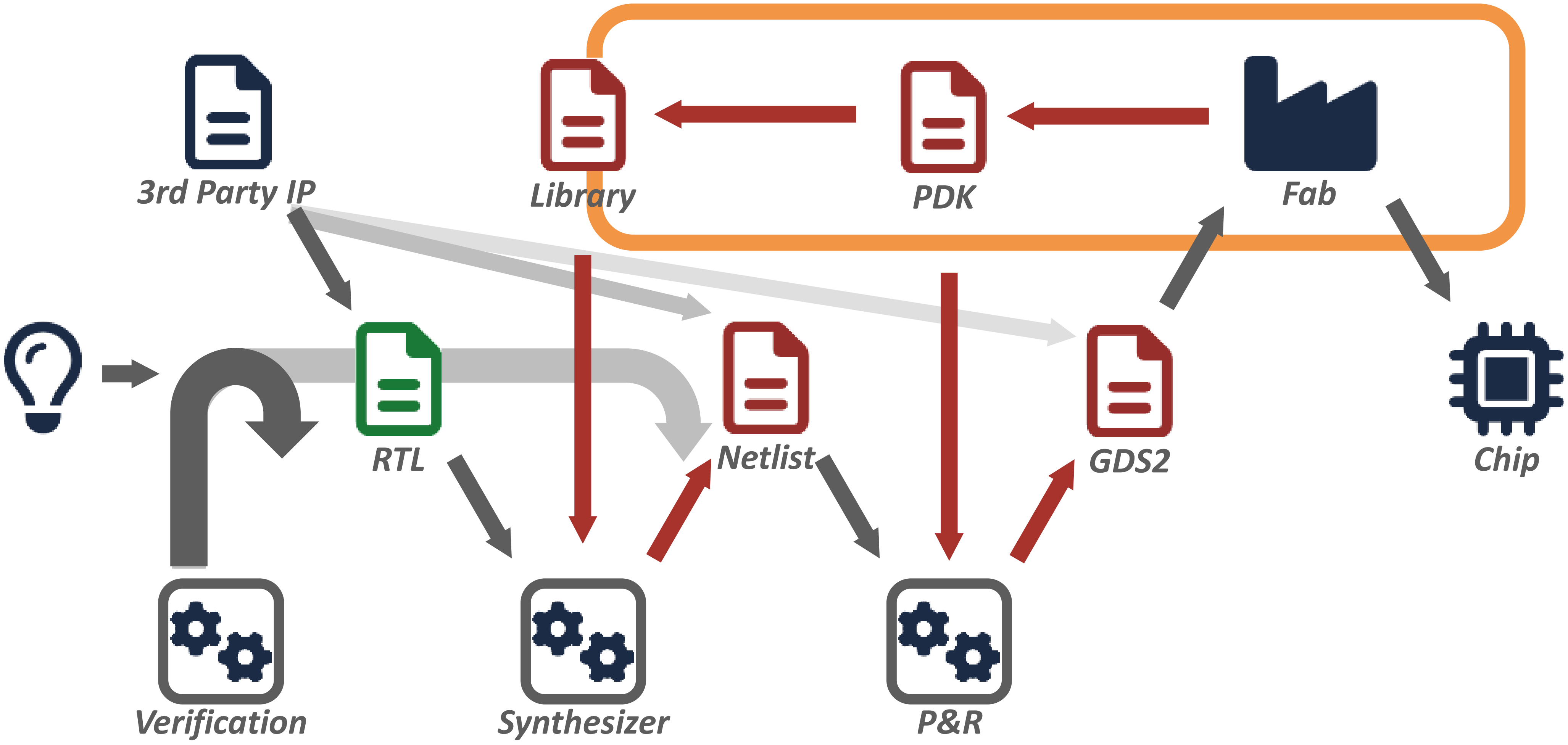
Simplified IC design flow: proprietary tools



EDA vendors limit the output of their tools

Icons taken from free icons from fontawesome.com

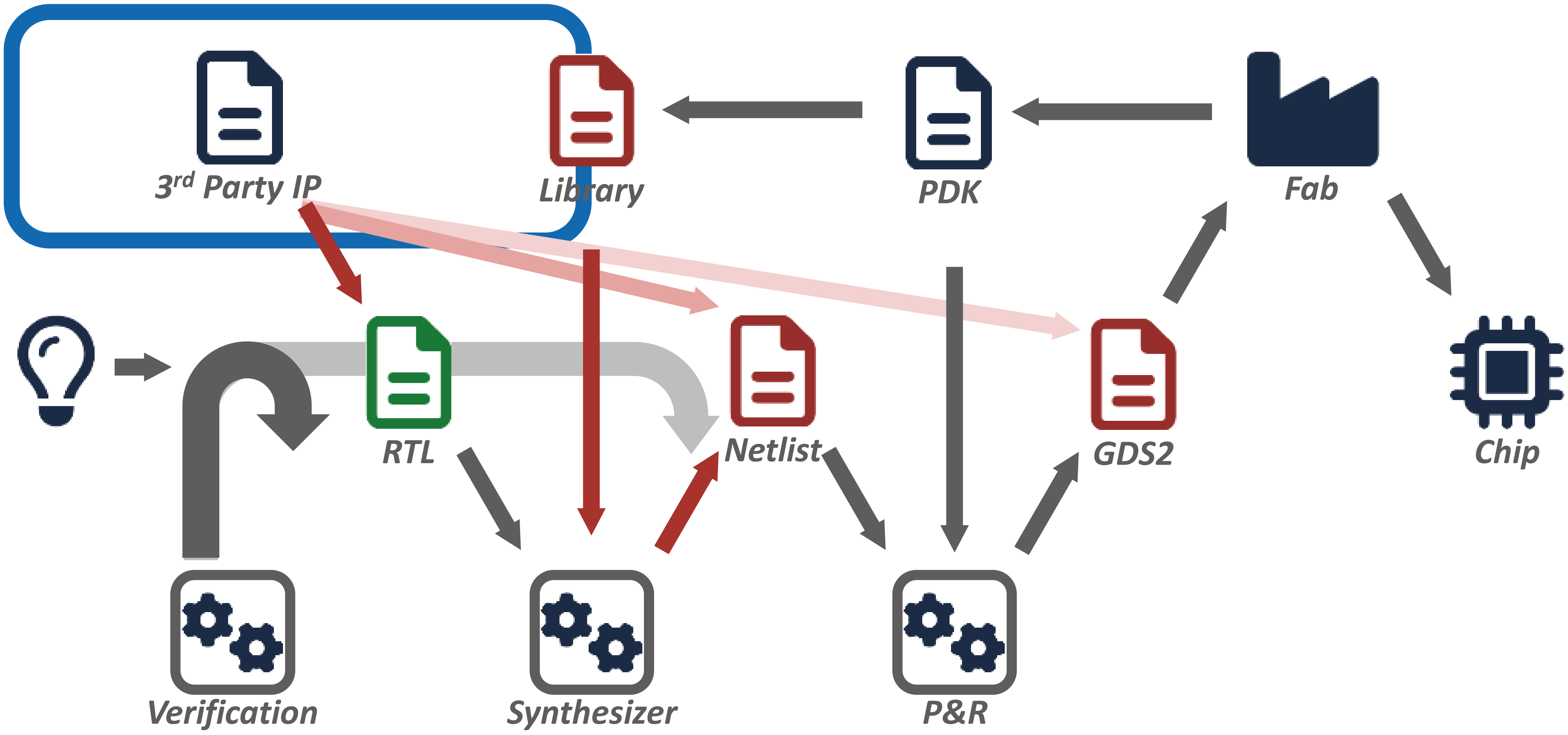
Simplified IC design flow: technology provider



Fabs do not make PDK information accessible

Icons taken from free icons from fontawesome.com

Simplified IC design flow: 3rd party IP



3rd party IP when included can limit what can be open sourced

Icons taken from free icons from fontawesome.com

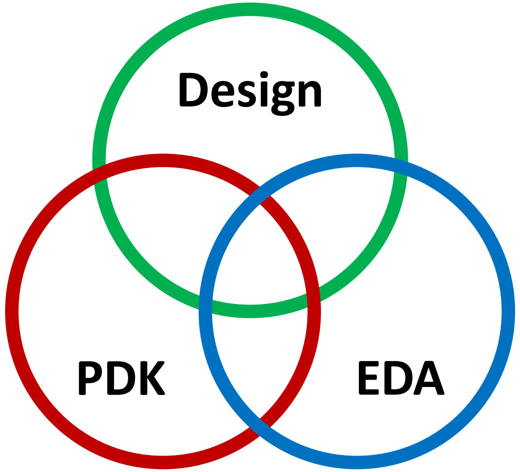
End-to-end open-flow aims to open all steps of IC design

Design

- RTL / HDL descriptions (quite common)
- Schematics / Physical Design (may have dependencies to technology information)

Tools (EDA)

- Front-end tools (Synthesis)
- Back-end tools (Placement and Routing)
- Verification tools (Simulation)



Manufacturing (PDK)

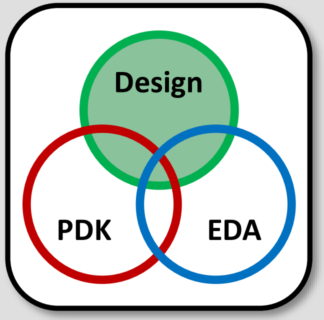
- Design rules for manufacturing (separation, minimum width of metals)
- Layer stack information for parasitics (thickness, dielectric constants..)
- Device models (SPICE parameters) for simulation

And I want to talk about why I believe end-to-end open flows are important

Notice that open parts in IC flow are independent

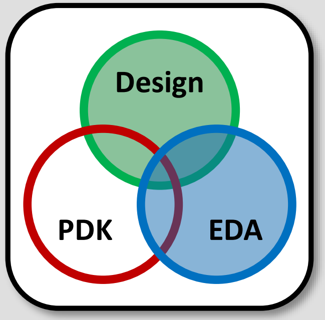
It is possible to use **open design** with closed EDA and closed PDK

(Picobello, Flamingo)



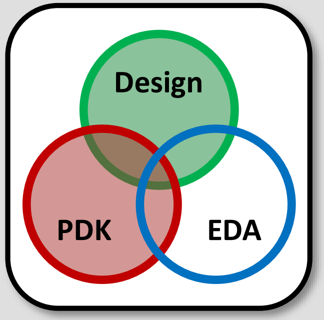
Or have **open designs** using **open EDA** on a closed PDK

(SeyrITA)



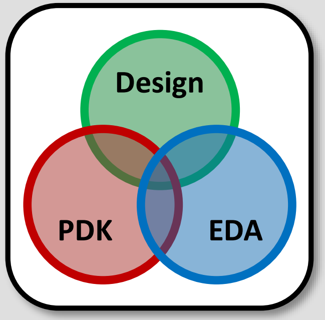
As well as having **open designs** using commercial EDA with **open PDKs**

(EZ Library)



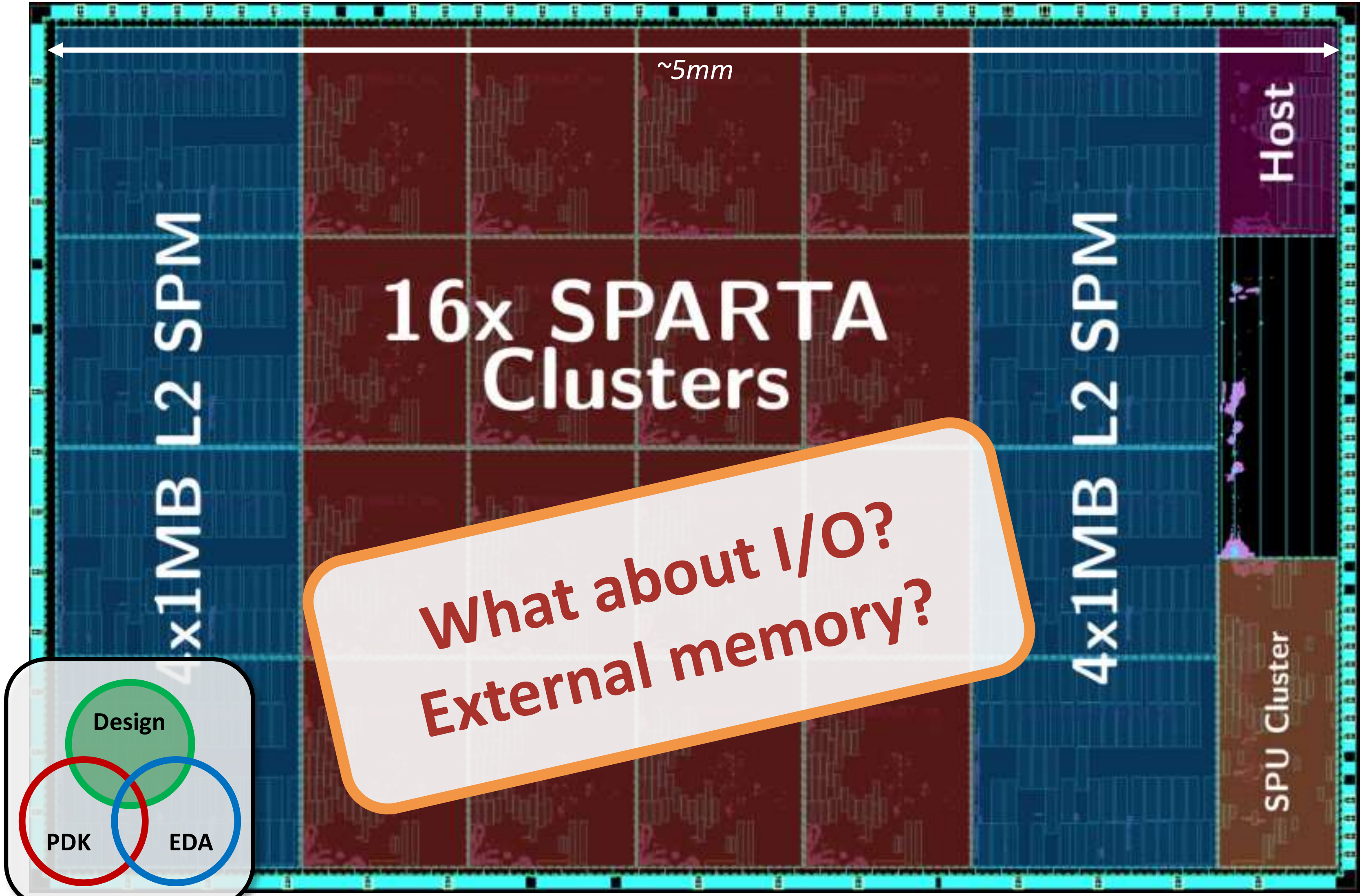
But end goal is to allow **open designs** using **open EDA** and **open PDKs**

(Basilisk, Mlem, Koopa)

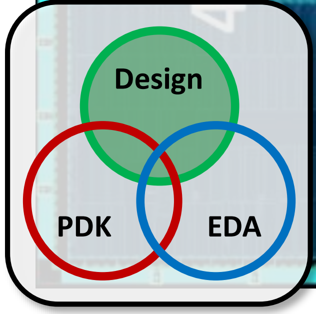


Of course combinations with closed designs are also possible, but these do not interest me so much ☺

Here is Picobello: our latest design in TSMC 7nm



What about I/O? External memory?



- 16 SPARTA clusters totaling 144x RISC-V cores with FP8-FP64-bit support
- 8x 1MB of on-chip L2
- Linux capable CVA6 Host
- Peripherals (JTAG, SPI, I2C)
- Running at 1+ GHz (WC), > 256 GFLOP/s (FP64) > 2 TFLOP/s (FP8)
- Tape-out August 2025
- Part of the EU Pilot project

You need help to make large modern SoCs

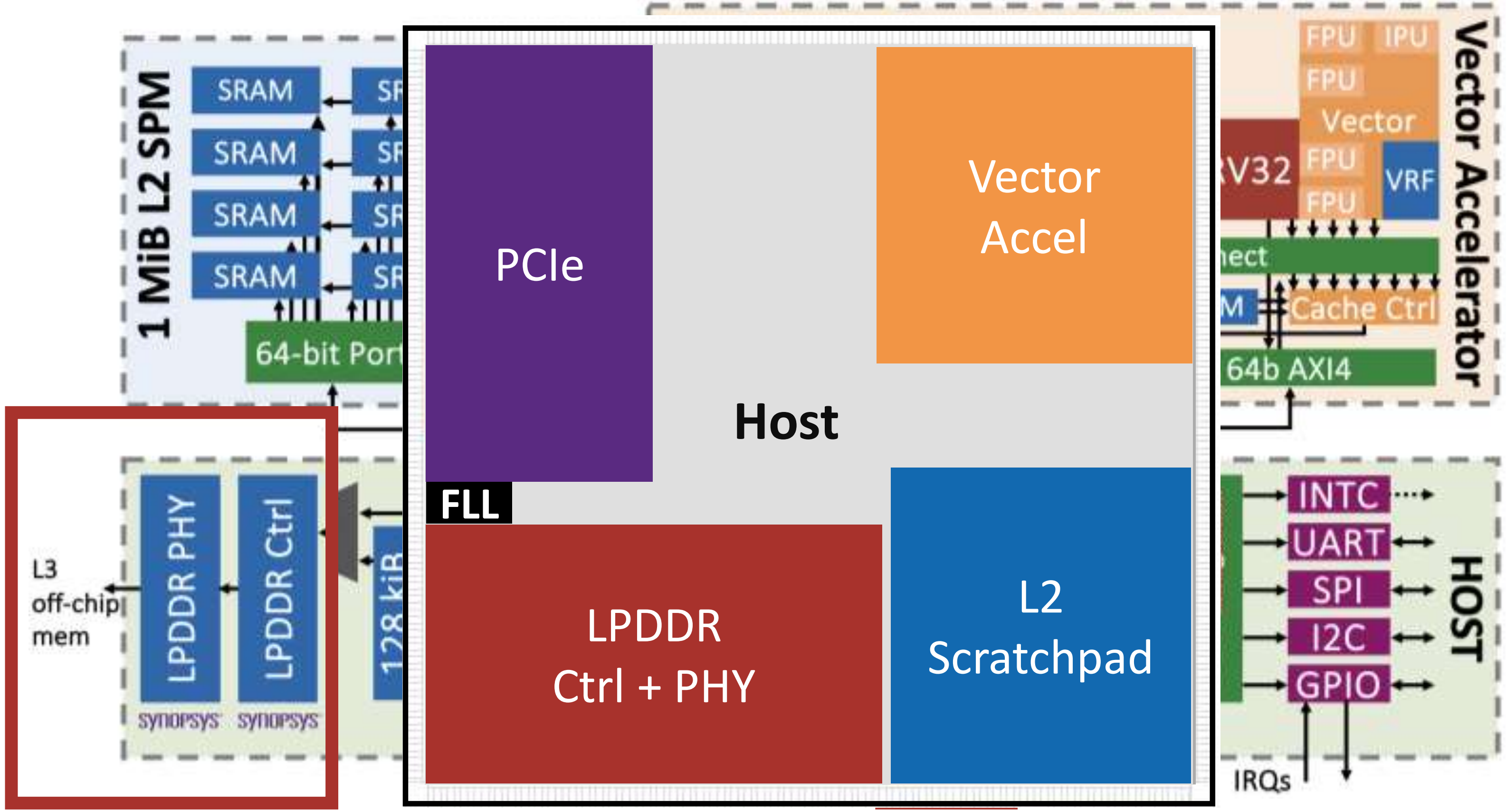
- **There are many innovative parts in Picobello**
  - Hopefully you will read about it in publications starting in 2026
- **But you can not afford to design all parts of an SoC from scratch by yourself**
  - **It builds on successful designs from the past**
    - CVA6 core : `https://github.com/openhwgroup/cva6`
    - Cheshire platform & peripherals : `https://github.com/pulp-platform/cheshire`
    - Snitch clusters : `https://github.com/pulp-platform/snitch_cluster`
    - FlooNoc : `https://github.com/pulp-platform/floonoc`
    - AXI : `https://github.com/pulp-platform/axi`
  - **Needs collaborations with experienced teams**
    - University of Bologna, TU-Munich

Supported by open-source designs in HDL

What about technology specific IPs? DDR, PCIe?

Finding such IP is not easy, you need great partners

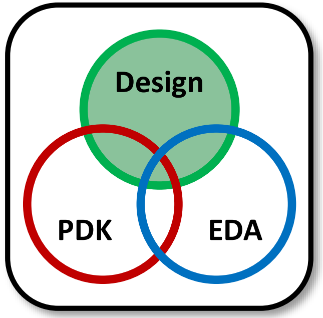
- **Meet Flamingo**
  - SoC with Vector based accelerator for AI applications in GF22



We would like to emphasize that this floorplan is not drawn to scale

GlobalFoundries™

- **EDA support by SYNOPSYS®**
- **Interface IP DDR / PCIe by SYNOPSYS®**



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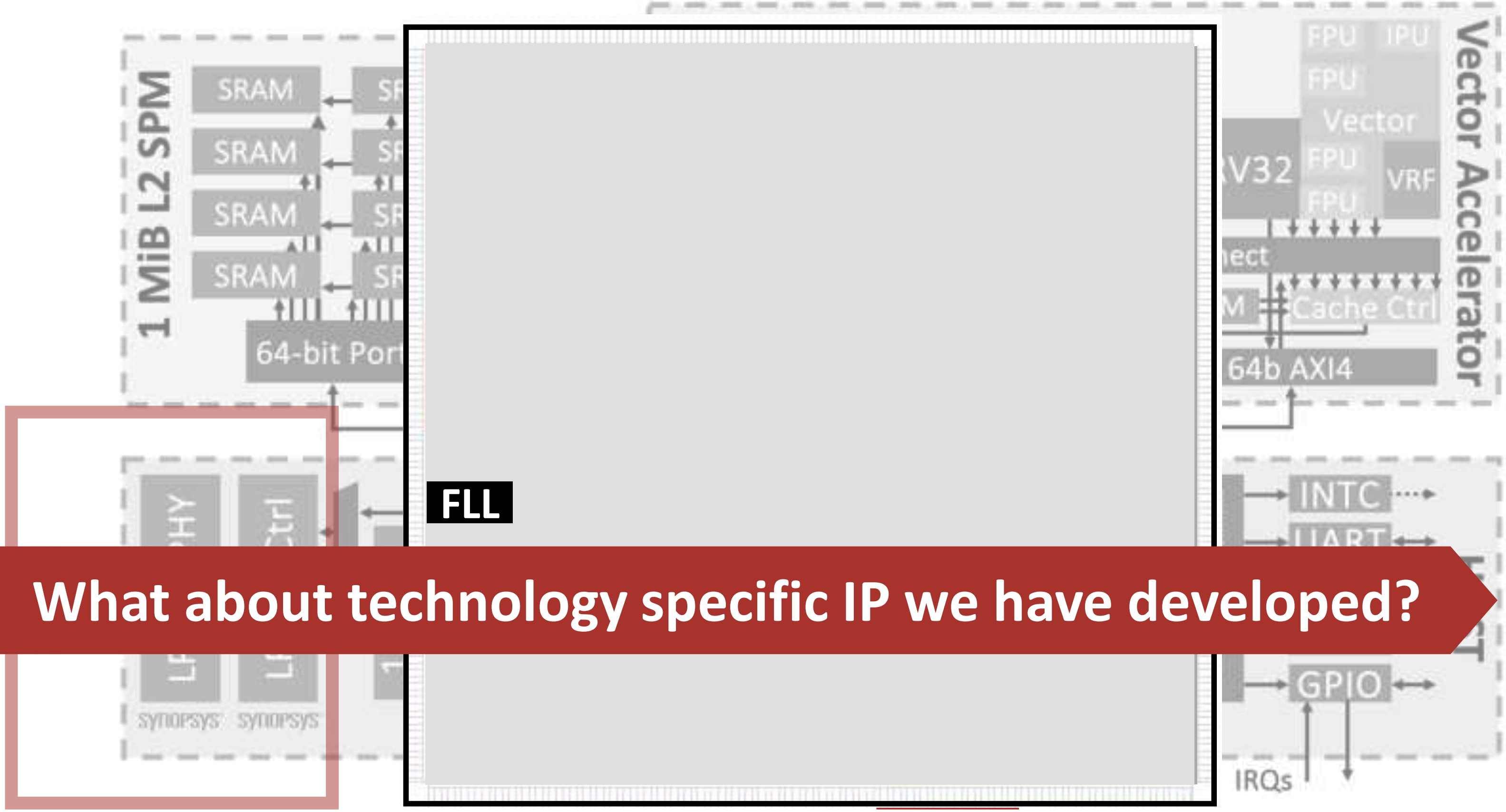
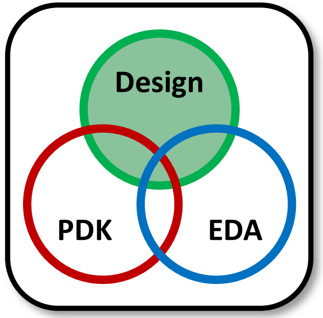


What about technology specific IP we have developed?

We would like to emphasize that this floorplan is not drawn to scale

GlobalFoundries™

- EDA support by SYNOPSYS®
- Interface IP DDR / PCIe by SYNOPSYS®



Sharing our FLL with others that need it

- **When you start designing in more modern technologies clock rates increase**
  - For 28nm and less clock rates of 500MHz – 2GHz are easily possible
  - It is difficult to bring such clocks externally, an internal clock generator could help
  - Good luck getting access to a low-cost clocking IP ☺
- **We designed an FLL (Frequency Locked Loop) back in 2016**
  - D. E. Bellasi and L. Benini, "Smart Energy-Efficient Clock Synthesizer for Duty-Cycled Sensor SoCs in 65 nm/28nm CMOS," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2322-2333, Sept. 2017, doi: 10.1109/TCSI.2017.2694322.
  - Ported and taped-out in many technologies: UMC65, TSCM65, GF22, GF12, TSMC7…

People have asked us repeatedly if we could share our FLL

.. and we really want to share our FLL, we know how much it helped us

Issues of sharing technology specific IP (like our FLL)

- **Assuming you have no objections from your own institution to share your IP**

The design requires technology data that is under NDA

- You can not share anything without getting permission from the technology provider
- Usually this requires a multi-party NDA

Your design may contain standard cells that come from a different provider

- You will have to contact the IP provider to ask for permission
- Our FLL for GF22 uses INVECAS standard cell libraries now owned by Synopsys
- In theory you can send a design WITHOUT the cells only references, and add the cells locally

You have used EDA tools with academic licenses for your design

- Most academic license agreements would not allow you to transfer the output to others
- You need to contact the EDA vendor and ask for their permission to share

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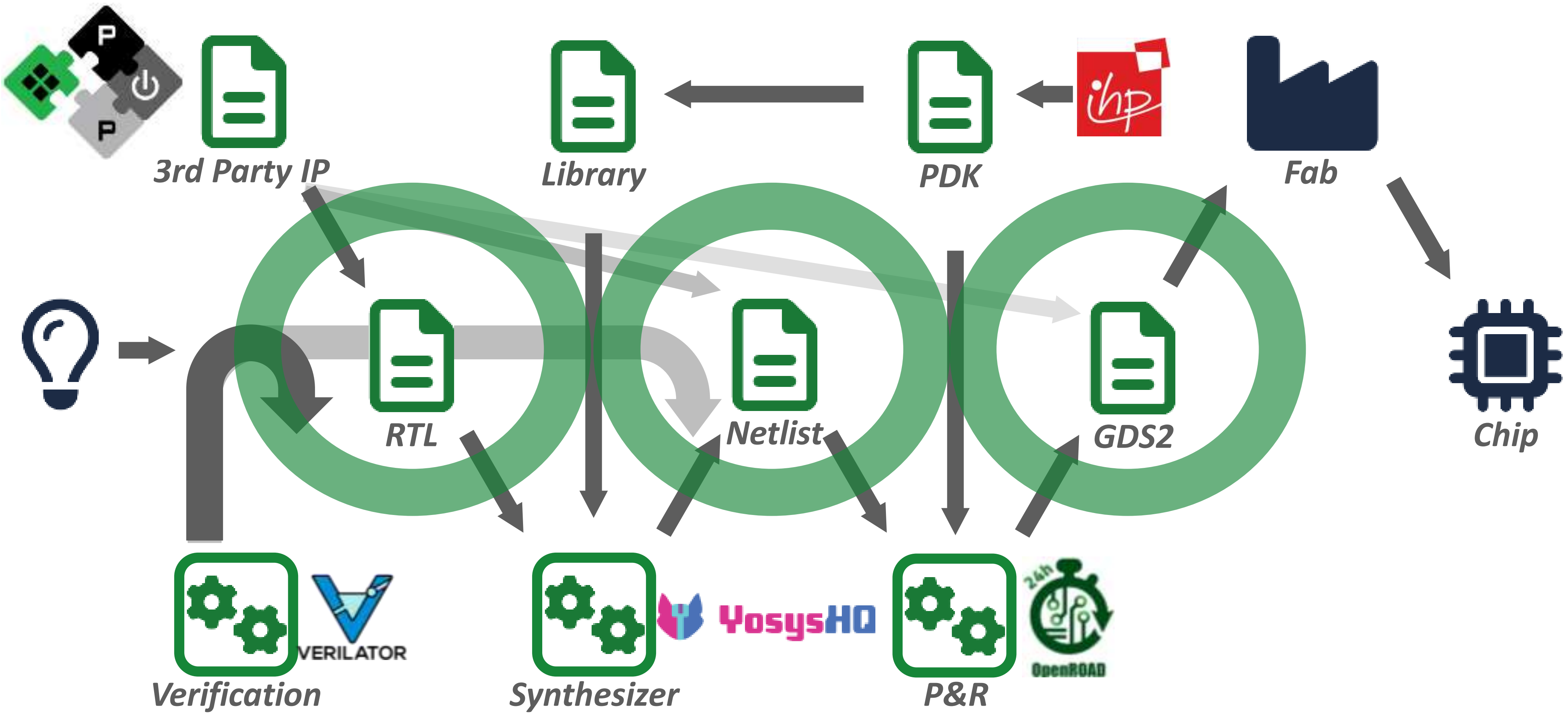
- o share

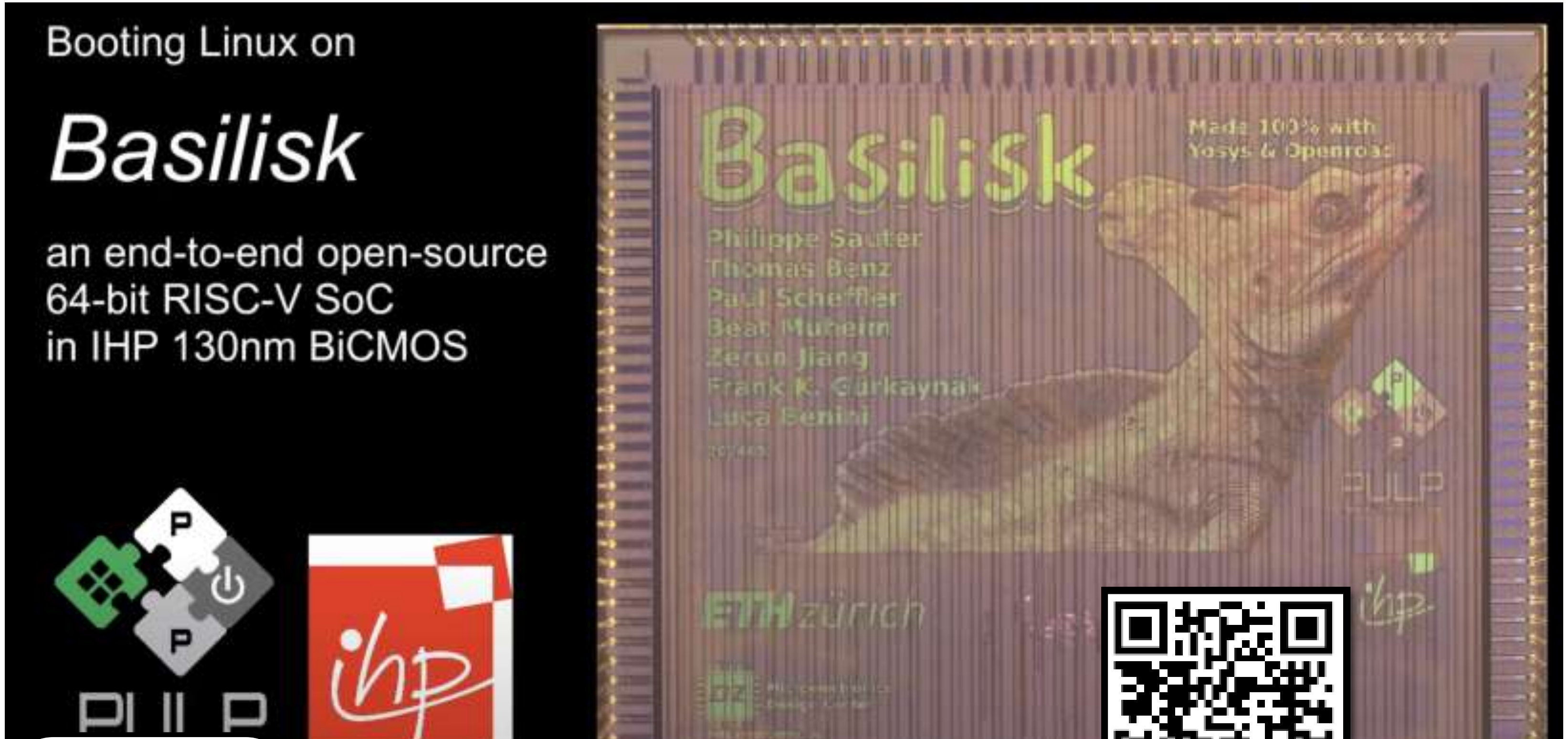
These things take a loooong time and are very tedious!

Process underway to share it with
TU-Braunschweig
TU Eindhoven
Boston University
Since 10th of January 2025 !

End-to-end Open-Source flow would help share IP



Meet Basilisk: End-to-end open SoC booting Linux



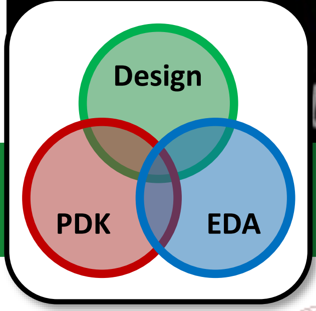
Booting Linux on

Basilisk

an end-to-end open-source 64-bit RISC-V SoC in IHP 130nm BiCMOS

Watch the video

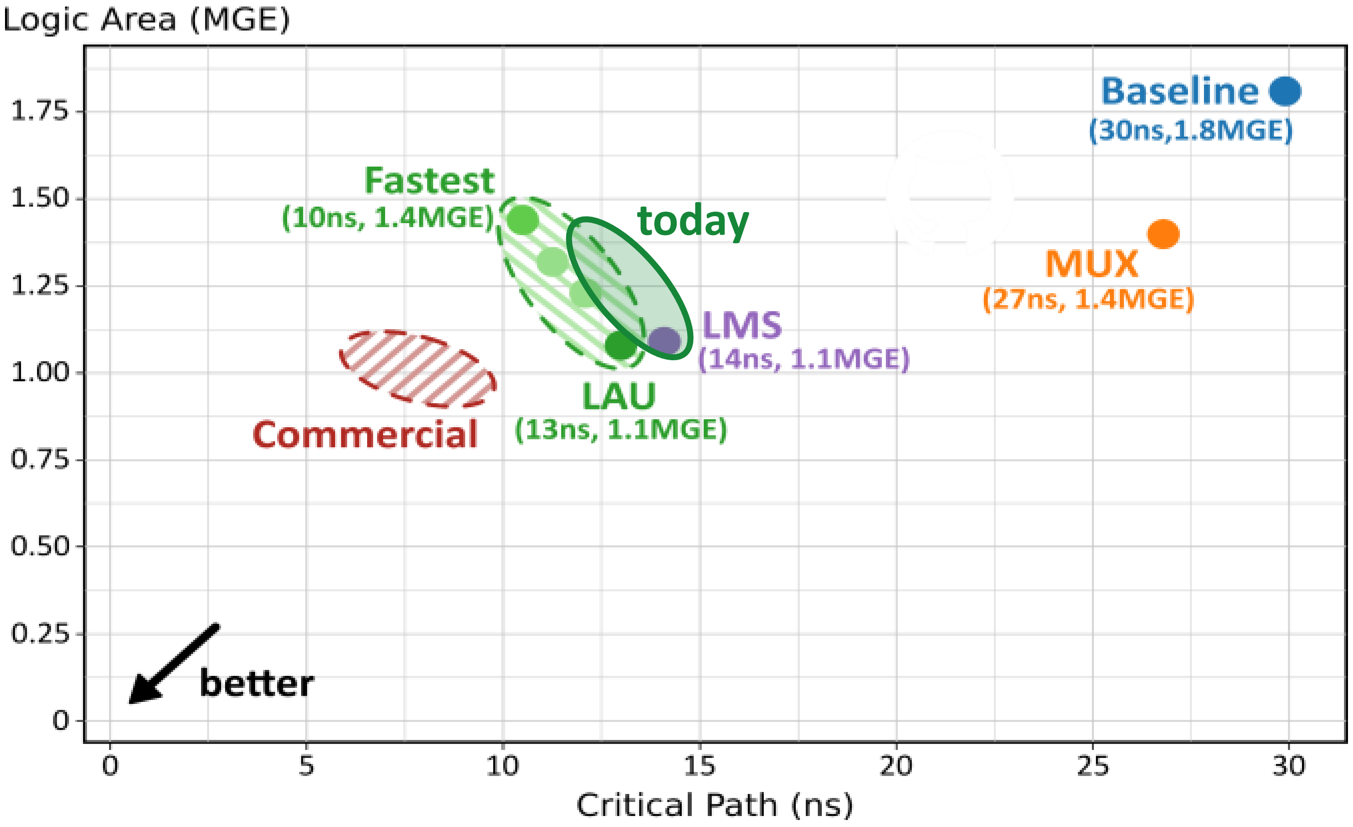
- **Open Design**
  - Cheshire with CVA6
- **Open EDA**
  - Yosys (with –slang)
  - OpenROAD
  - KiCAD (for board)
- **Open PDK**
  - IHP 130
  - Open standard cells
  - Memory macros



github.com/pulp-platform/cheshire-ihp130-o

Working with open-source EDA groups to close the gap!

- **Improvements until June 2024**
  - SV-to-Verilog chain @ **<2min** runtime
  - Yosys synthesis:
    → **1.1 MGE** (**1.6×**) @ **77 MHz** (**2.3×**)
    → **1.4×** less runtime, **2.4×** less peak RAM
  - OpenROAD P&R: tuning
    → **-12%** die area, **+10%** core utilization
- **Improvements June-October**
  - Yosys-slang replaces SV2V
    - **1.6×** less runtime, **10×** less peak RAM
  - **-10%** logic area (preliminary)

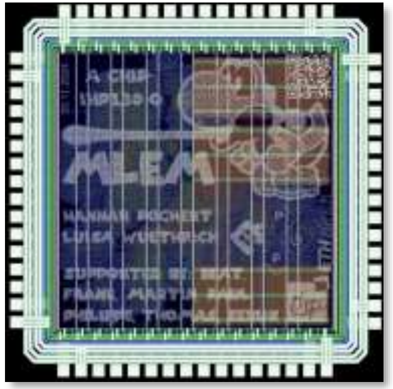


There is still a gap to commercial tools, but it is much less than you think it is

At ETH Zürich, IC Design teaching uses open source HW

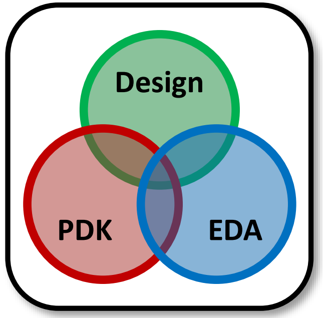
- **Starting 2025, our IC Design course switched to (mostly) open source**
  - Using IHP 130, Yosys and OpenROAD
    - Parts for backannotated simulation, test pattern generation, DRC/LVS, still use proprietary tools
- **Exercises based on a 32bit RISC-V microcontroller we call Croc**

https://github.com/pulp-platform/croc



- **Project based grading**
  - Students (in groups of two) will have to modify the exercise design
  - Best five designs will be taped-out
- **Huge advantage:**
  - We can share lecture and exercise content with everyone

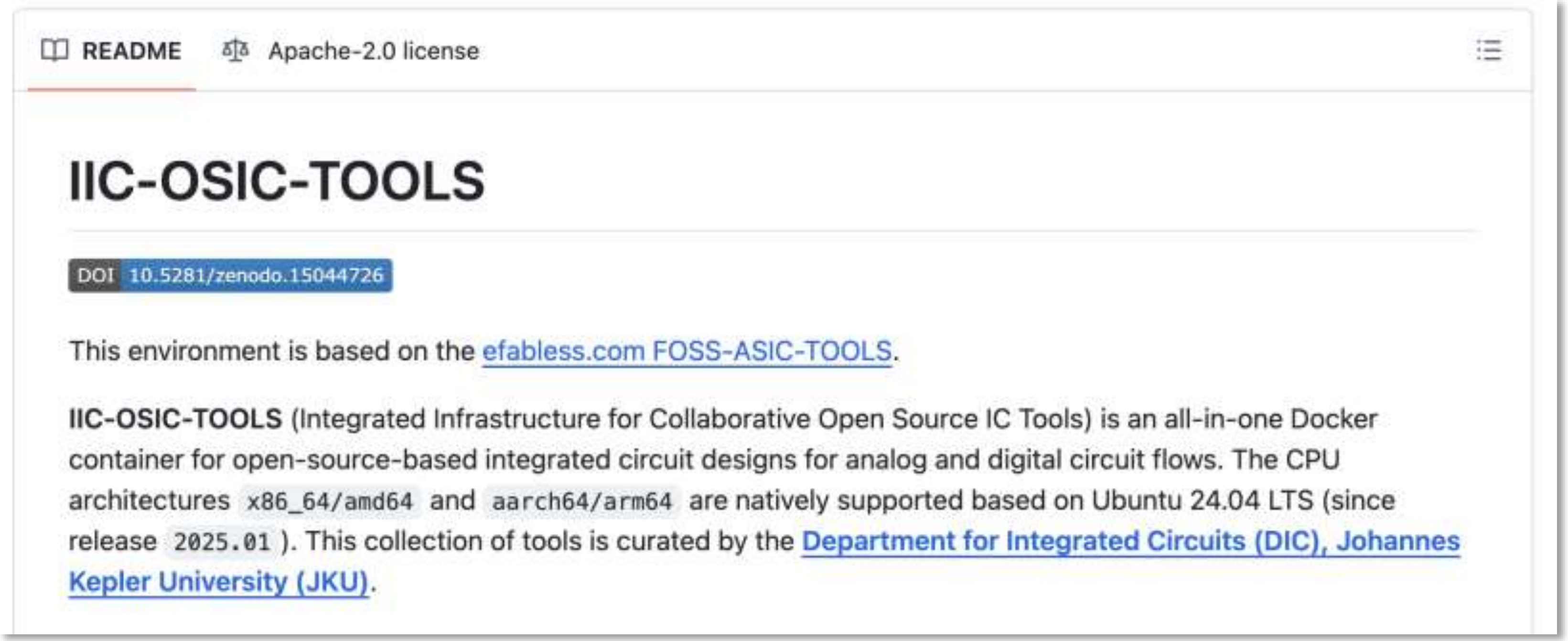
https://vlsi.ethz.ch



Reliable collection of open source tools is essential!

- **Most open source developers have their own idea about the environment**
  - Getting several independent tools to work at the same time is very demanding work
  - Preparing/sharing lectures require you to be able to point to a reliable image

`https://github.com/iic-jku/IIC-OSIC-TOOLS` to the rescue



IIC-OSIC-TOOLS

DOI 10.5281/zenodo.15044726

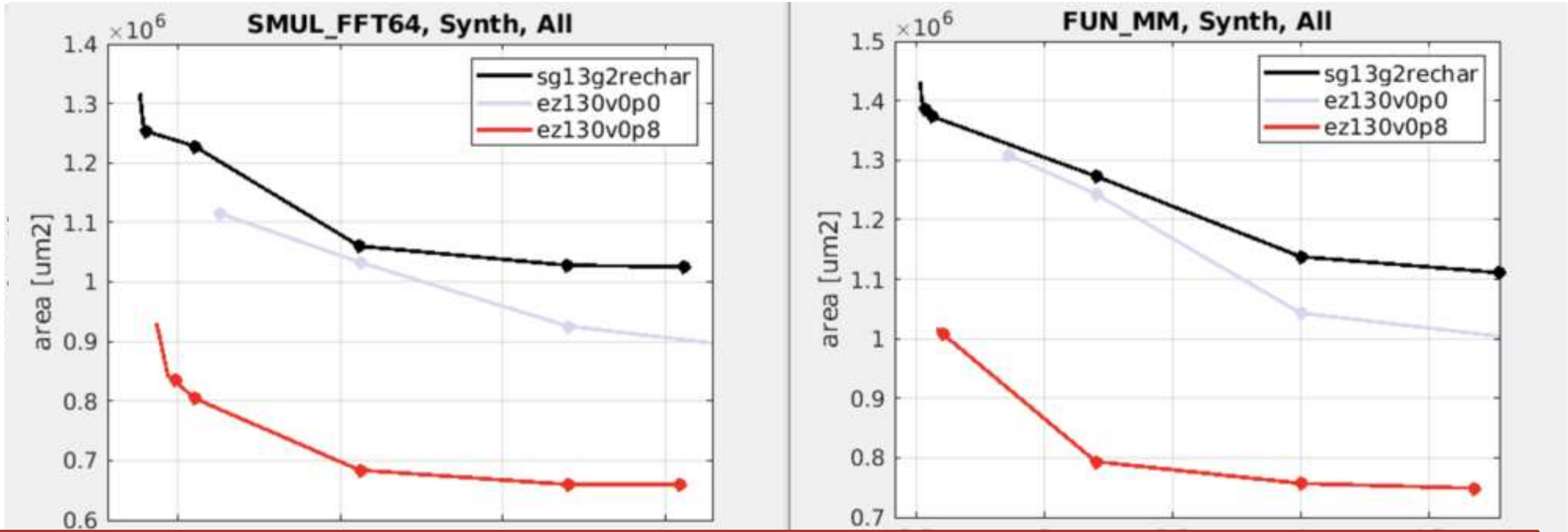
This environment is based on the efabless.com FOSS-ASIC-TOOLS.

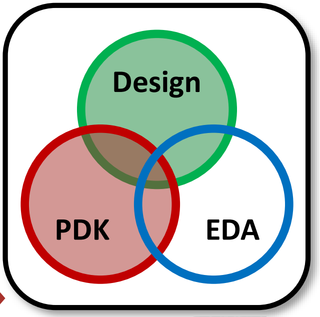
IIC-OSIC-TOOLS (Integrated Infrastructure for Collaborative Open Source IC Tools) is an all-in-one Docker container for open-source-based integrated circuit designs for analog and digital circuit flows. The CPU architectures `x86_64/amd64` and `aarch64/arm64` are natively supported based on Ubuntu 24.04 LTS (since release `2025.01`). This collection of tools is curated by the Department for Integrated Circuits (DIC), Johannes Kepler University (JKU).

Thanks Harald ☺

EZ Library: new standard cells for IHP130

- **VLSI 5 lecture by the Integrated Information Processing group at ETH Zürich**
  - By Oscar Castañeda Fernández, Christoph Studer and a bit of support from me
- **In one semester, 18 students re-designed a standard cell library for IHP130**

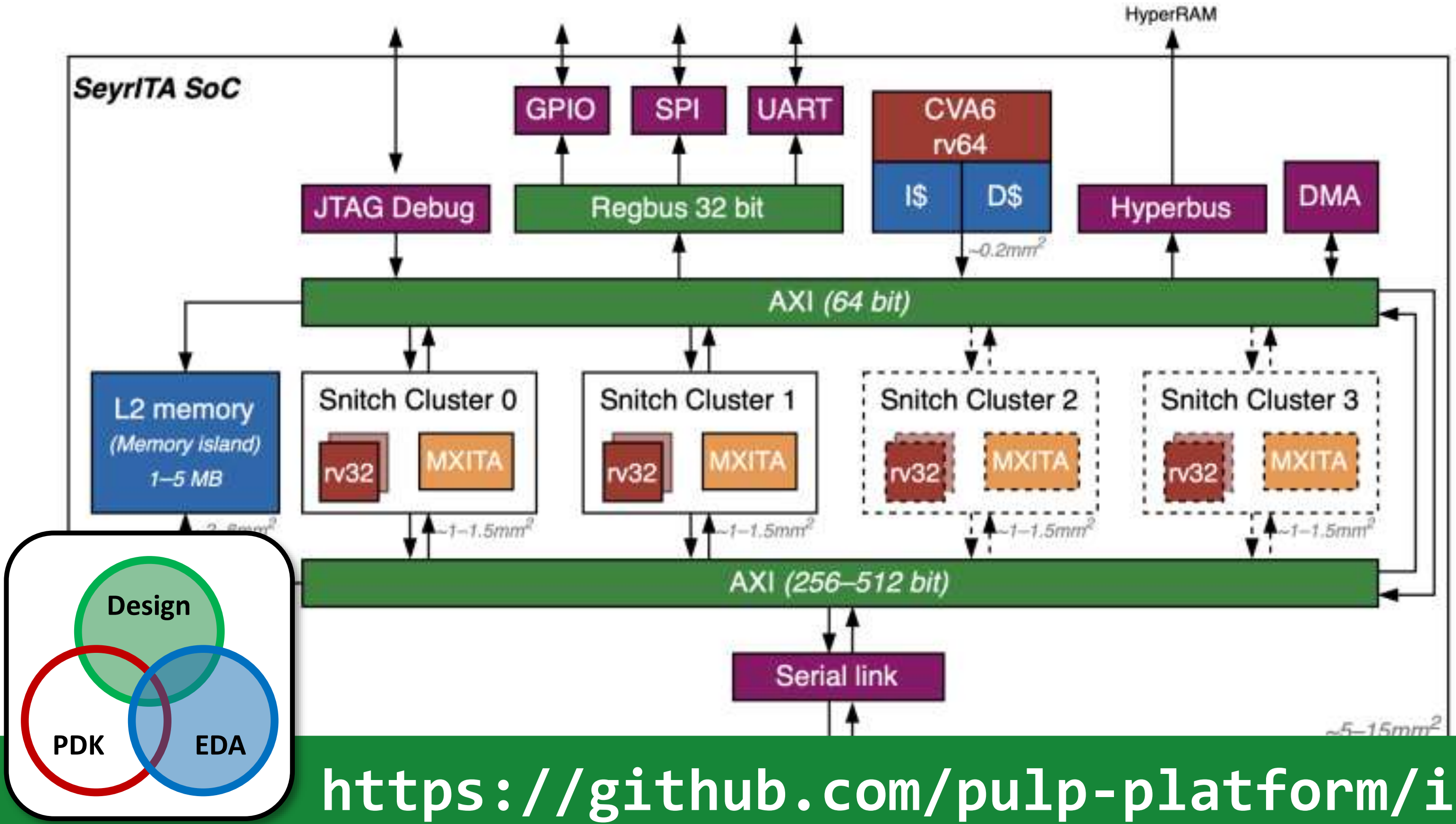




Unfortunately, we did not use open EDA, now I am having fun with legal

SeyrITA, our most ambitious project for embodied AI

- **Designing a research relevant SoC using open source EDA in GF22**
  - State of the art accelerator for embodied AI, using Integer Transformer Accelerator (ITA)
- **Collaborative open work with OpenROAD, Yosys**



- **Challenging work**
  - Large design, modern technology
  - We encounter problems daily
  - We try to solve them one problem at a time
  - Confident we will get it done
- **Target tape-out**
  - End of 2025 / Early 2026

https://github.com/pulp-platform/ita

There are still many challenges, our work is not done!

- **We need more open PDKs**
  - Something in the 65nm – 28nm range would be a **game changer**
  - Drafted an open letter to raise awareness with 300+ signatures

https://open-source-chips.eu/

- **Parts of open EDA already in good shape, but there are gaps**
  - Many independent groups are working on tools, need to support inter-operability
  - Possible EU funding for 20MEUR for open source EDA development, project outline submitted
  - Opportunity to go beyond what standard tools are able to deliver, close the PPA gap!
- **End-to-end open source design requires set of IPs that others can use**
  - Memories, Serial I/O, Data converters, Memory controllers, PHYs for common protocols
  - List is long, we will have enough work to do ☺

End-to-end Open-Source IC Design is already working!

It will only get better

Easier collaboration / sharing

- Need to stand on the shoulder of giants
- Share common parts that all need
- Concentrate work/time where it matters

Open reproducible results

- Everyone can verify performance claims
- Allows us to generate example datasets that can be used to train/improve tools

Innovation all over IC Design

- No longer limited to only design
- Improve design flows, design tools
- Create new opportunities

Accessible teaching for all

- Share courses, designs, examples
- Create tutorials, knowledge bases
- Lower entry barriers also for industry