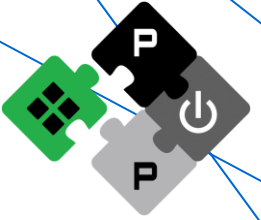

ASTRAL
A MIXED-CRITICALITY RISC-V SOC ARCHITECTURE FOR SATELLITE ONBOARD AI

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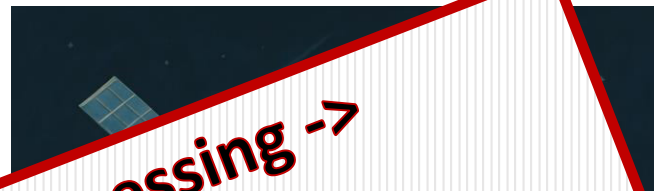
AI IN SPACE CYBER-PHYSICAL SYSTEMS (SATELLITES)

Autonomous operations [1]

- Orbital collision hazard avoidance
- Asset reconfiguration
- Dynamic mission planning and reconfiguration [2]



Real-time edge data processing -> Computing power

Fault Tolerance and Reliability

Research (industrial/academic) -> Open platforms

erstanding

tion for

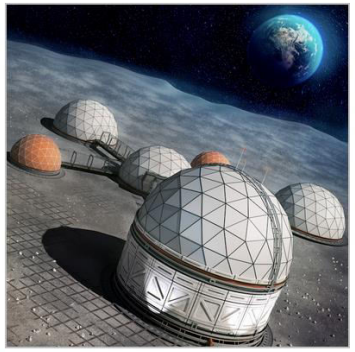
esat for AI cloud detection

ng [4]

Fault detection, Isolatio

Recovery (**FDIR**) [5]

RISC-V FOR APPLICATIONS IN SPACE



January 30, 2023

NASA Recruits Microchip, SiFive, and RISC-V to Develop 12-Core Processor SoC for Autonomous Space Missions

by Steven Leibson

NASA's JPL (Jet Propulsion Lab) has selected Microchip to design and manufacture the multi-core High Performance Spaceflight Computer (HPSC) microprocessor SoC based on eight RISC-V X280 cores from SiFive with vector-processing instruction extensions organized into two clusters, with four additional RISC-V cores added for general-purpose computing. The project's operational goal is to develop "flight computing technology that will provide at least 100 times the computational capacity compared to current spaceflight computers." During a talk at the recent RISC-V Summit, Pete Fiacco, a member of the HPSC Leadership Team and JPL Consultant, explained the overall HPSC program goals.

RISC-V®

IN SPACE

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RISC-V IN SPACE

Workshop April 2-3, 2025 | Gothenburg

RISC-V in Space

Lack of open platforms to speed up academic and industrial research for space

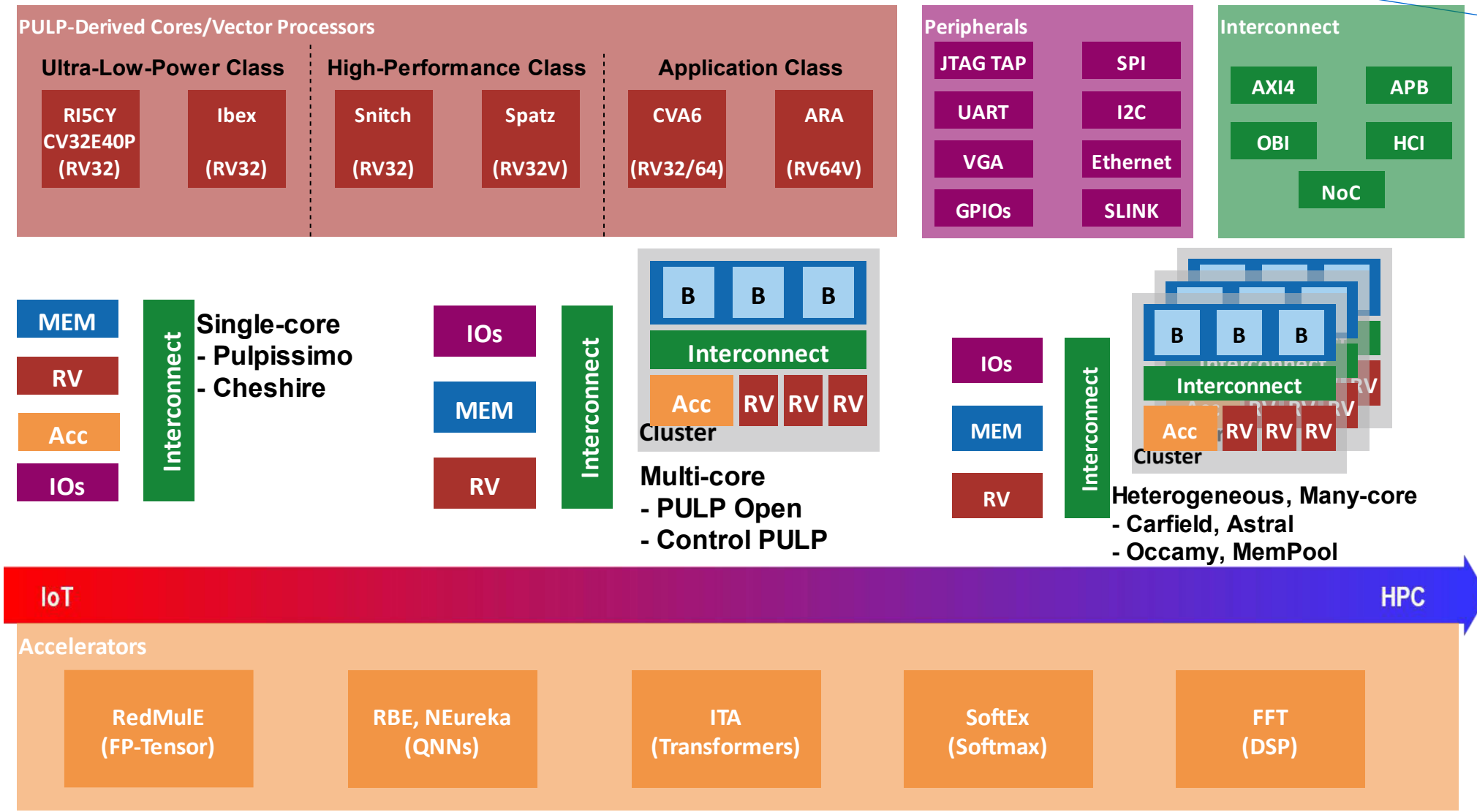
https://github.com/pulp-platform

THE PULP TEAM

Wide research team spread across University of Bologna and ETH Zurich

https://pulp-platform.org/team.html

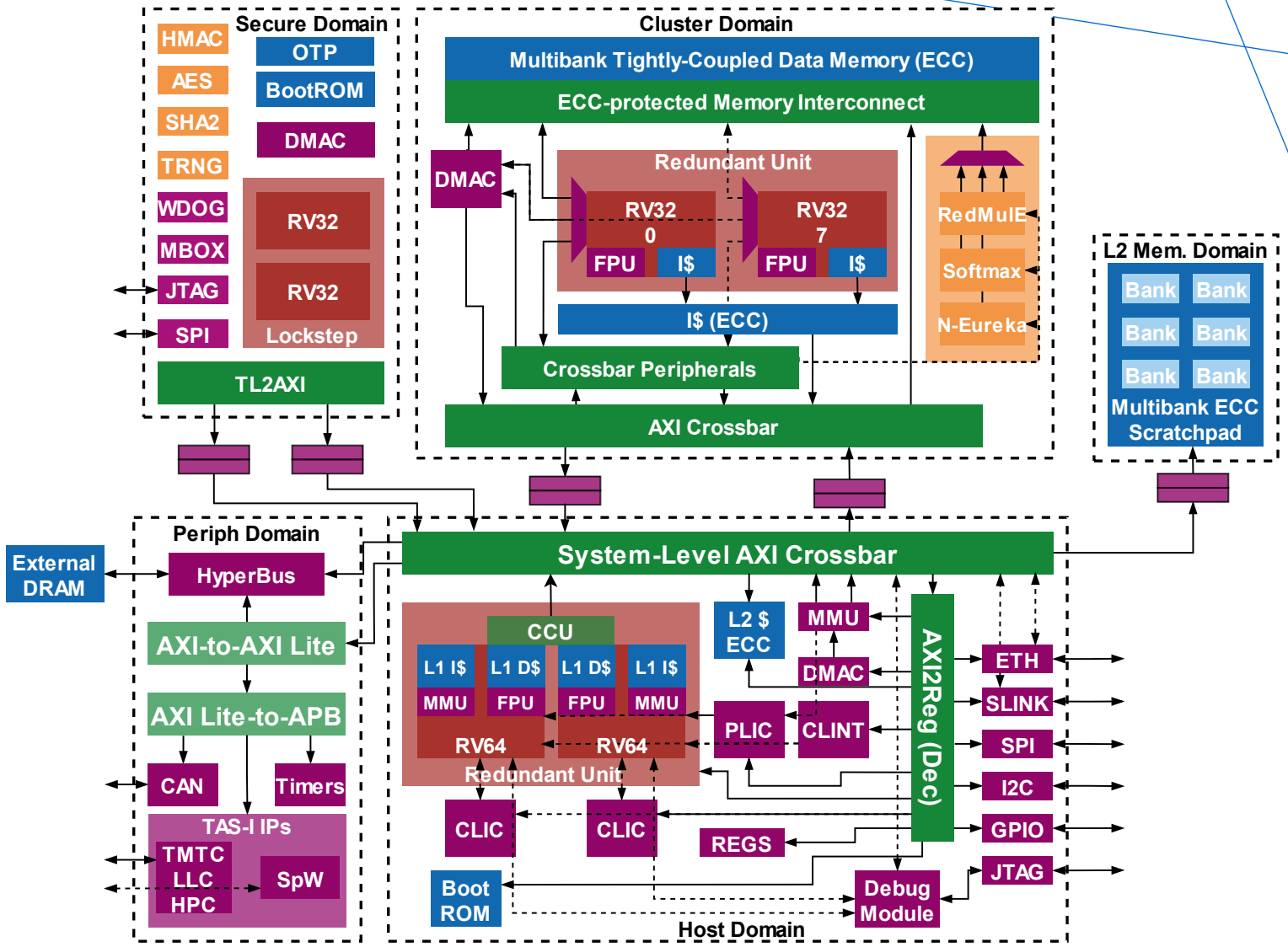
OPEN-SOURCE DIGITAL IPS AND SYSTEMS



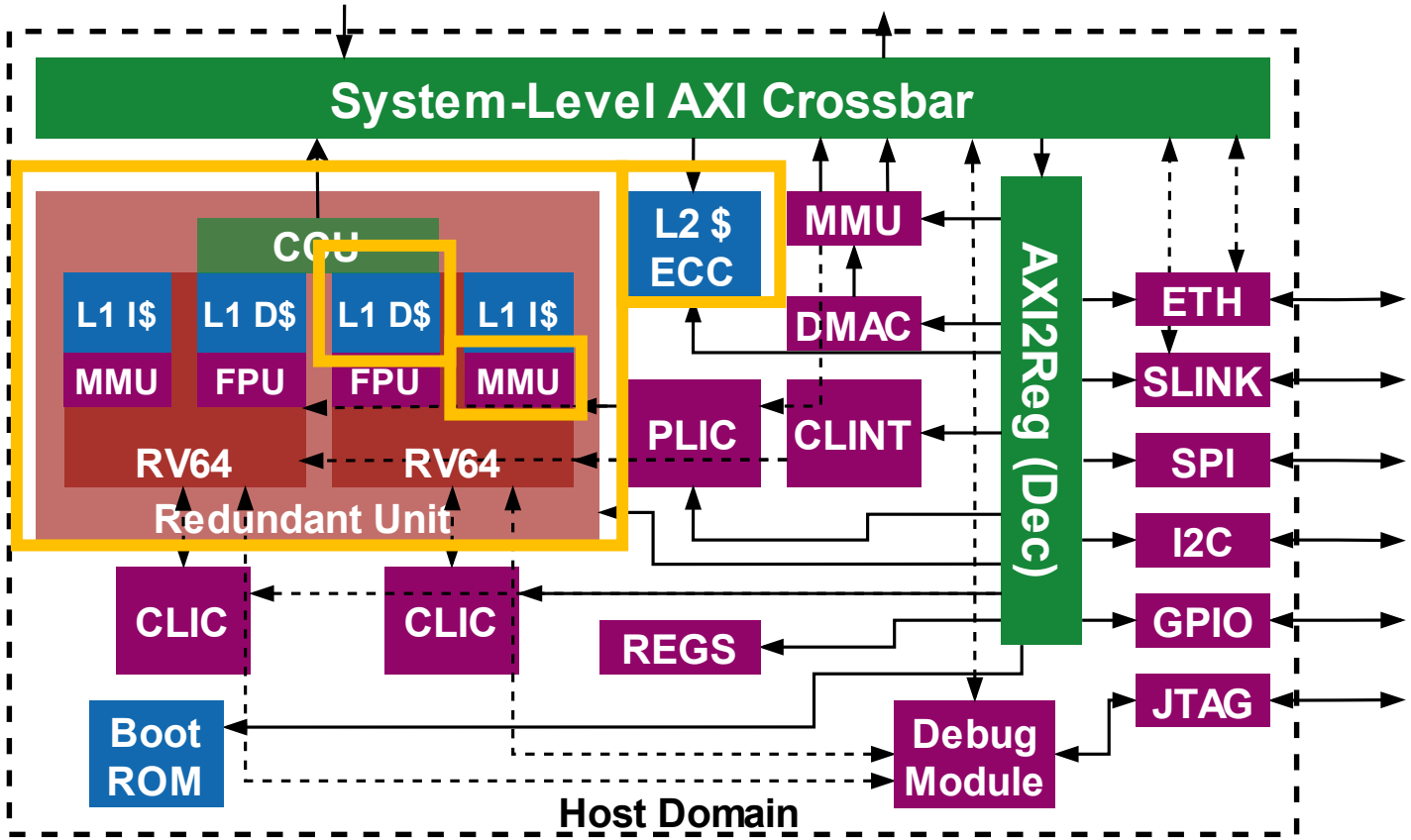
ASTRAL SOC – UNLEASH AI ACCELERATION IN SPACE

First-of-a-kind mixed-criticality heterogeneous platform

- **Fault tolerance** – architectural extensions for redundancy, error correction, and real-time recovery
- **Fully open-source** – all IPs are open-source and released under Apache-like license
- **Highly parametric** – straight-forward integration of additional IPs
- Ease of **programmability** – boots full-fledge Linux OS
- **Performance&Security** – powerful multicore accelerator + Root of Trust
- **Development - Plug&Play** flow for **AMD Xilinx Ultrascale+ VCU118**

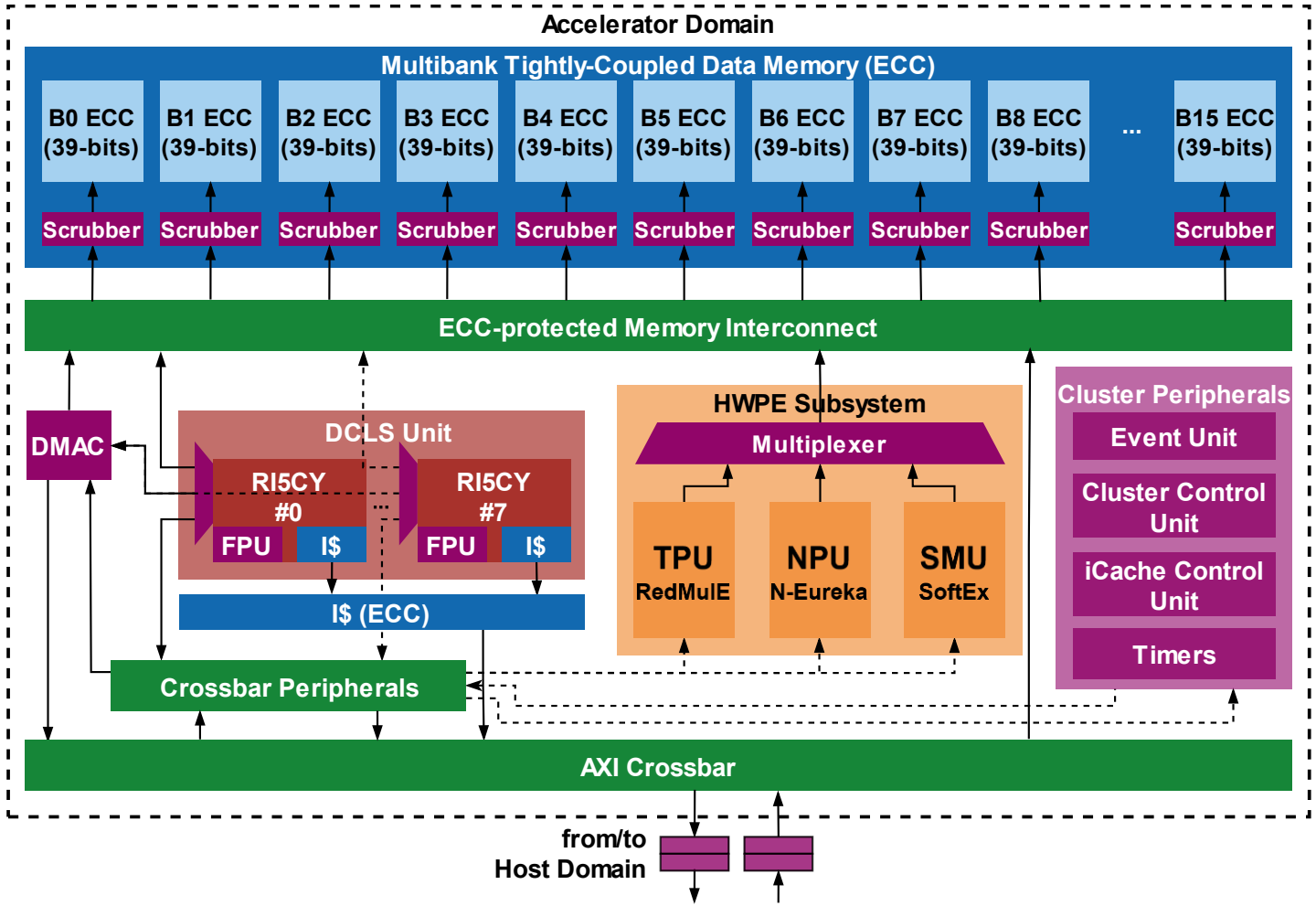


ASTRAL SOC – HOST DOMAIN ARCHITECTURE



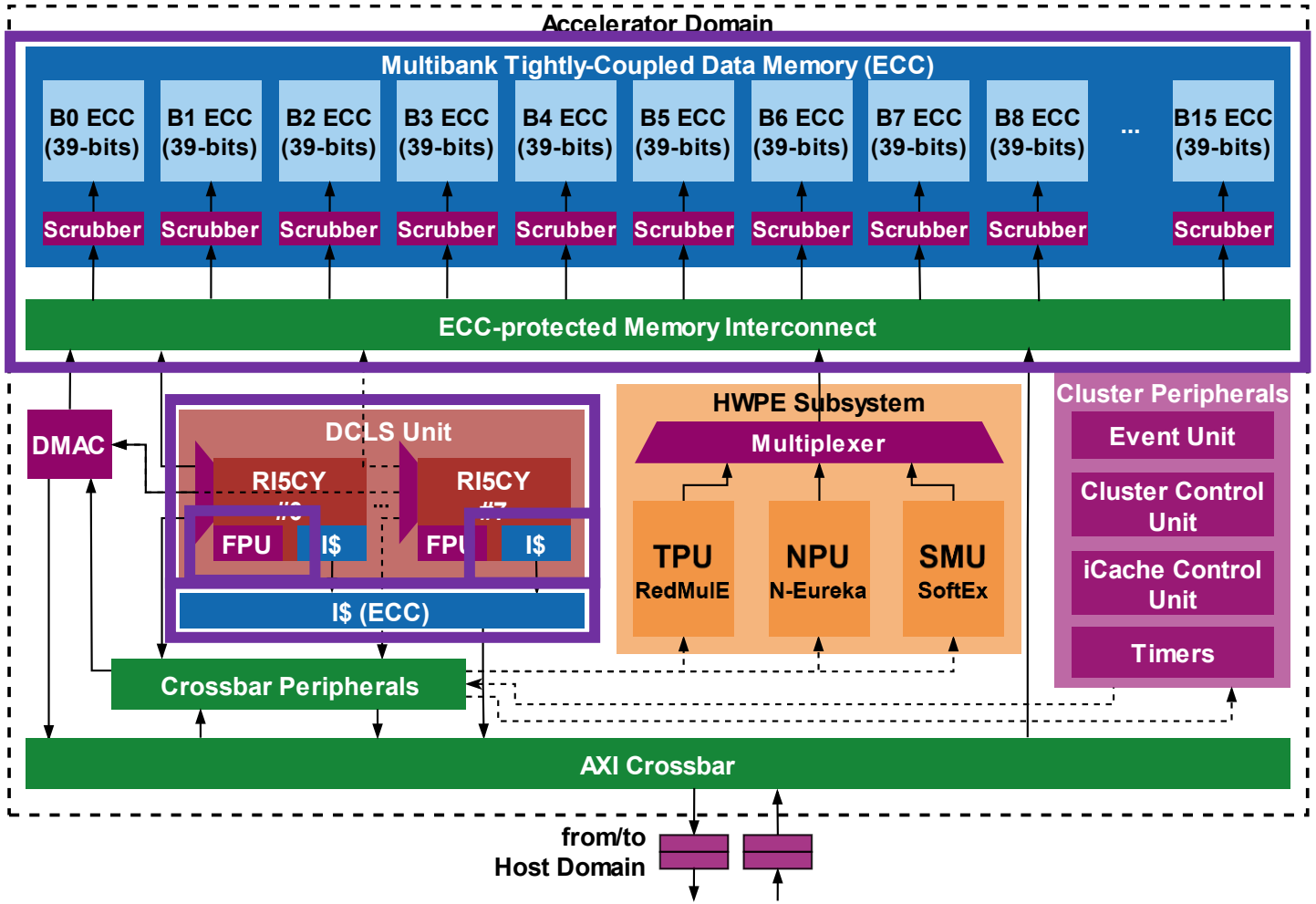
- **Linux-capable** multicore (1 - 4) cache-coherent cluster of **64-bit CVA6** cores based on the **ACE** protocol
- Runtime-programmable **redundant grouping** of the CVA6 cores to balance **reliability** and **performance**
  - **Less then 100 clock cycles fault recovery** with hardware extension
- **SEC-DED** extension of the CVA6 **TLB**s and **Branch Predictor**
- **ECC** extension of the **L1 data cache** of the cores for SECDED
- **ECC** extension of the **L2 cache** for single error automatic correction, and cache re-fetch/IRQ notification in case of multiple errors on clean/dirty lines

ASTRAL SOC – ACCELERATOR DOMAIN ARCHITECTURE



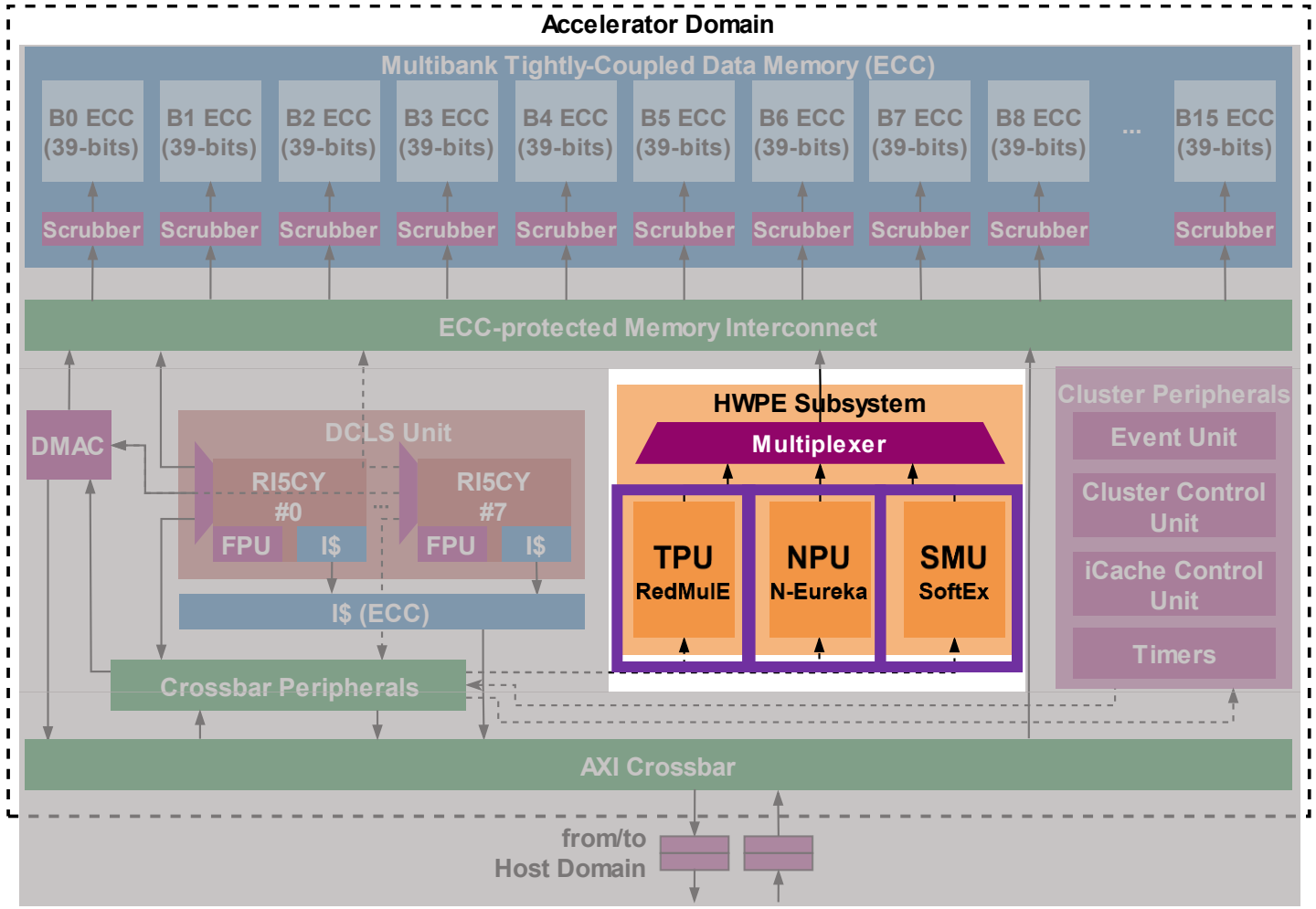
- 32-bit Octa-core cluster with DSP extensions for transprecision computing
- Shared multi-bank interleaved scratchpad memory + DMAC and peripherals

ASTRAL SOC – ACCELERATOR DOMAIN ARCHITECTURE



- Hybrid Modular Redundant cluster for runtime reconfiguration (**TMR/DMR/Independent**)
  - **Less then 30 clock cycles fault recovery** with hardware extension
- Extension of the cores' **FPU**s with **temporal repetition** with detection + correction of internal faults
- **L0 + L1 instruction cache** protected with **parity** for lines replacements in case of errors
- **Memory subsystem** protected with **SECDED** from the cores and accelerators branches down to the memory banks (storing ECCs) + memory **scrubbers**

ASTRAL SOC – ACCELERATOR DOMAIN ARCHITECTURE

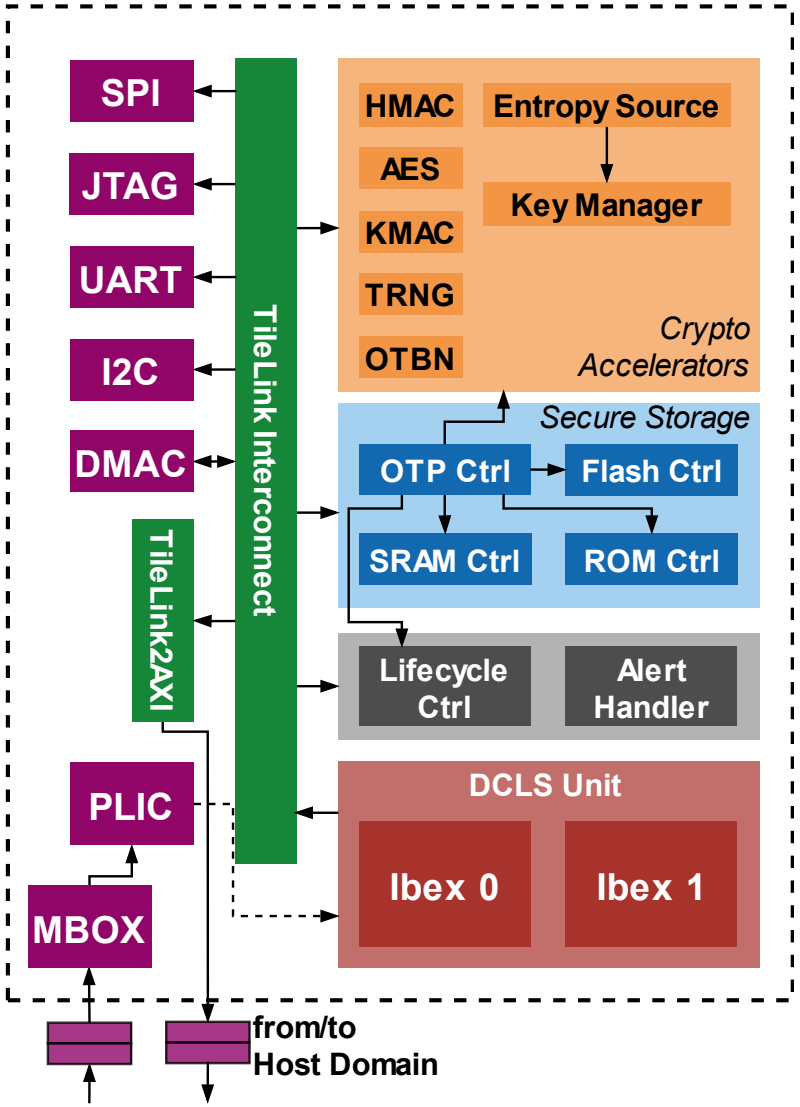


Coupling **performance** with **reliability**

Wide **accelerator subsystem** for on-chip inference and training acceleration

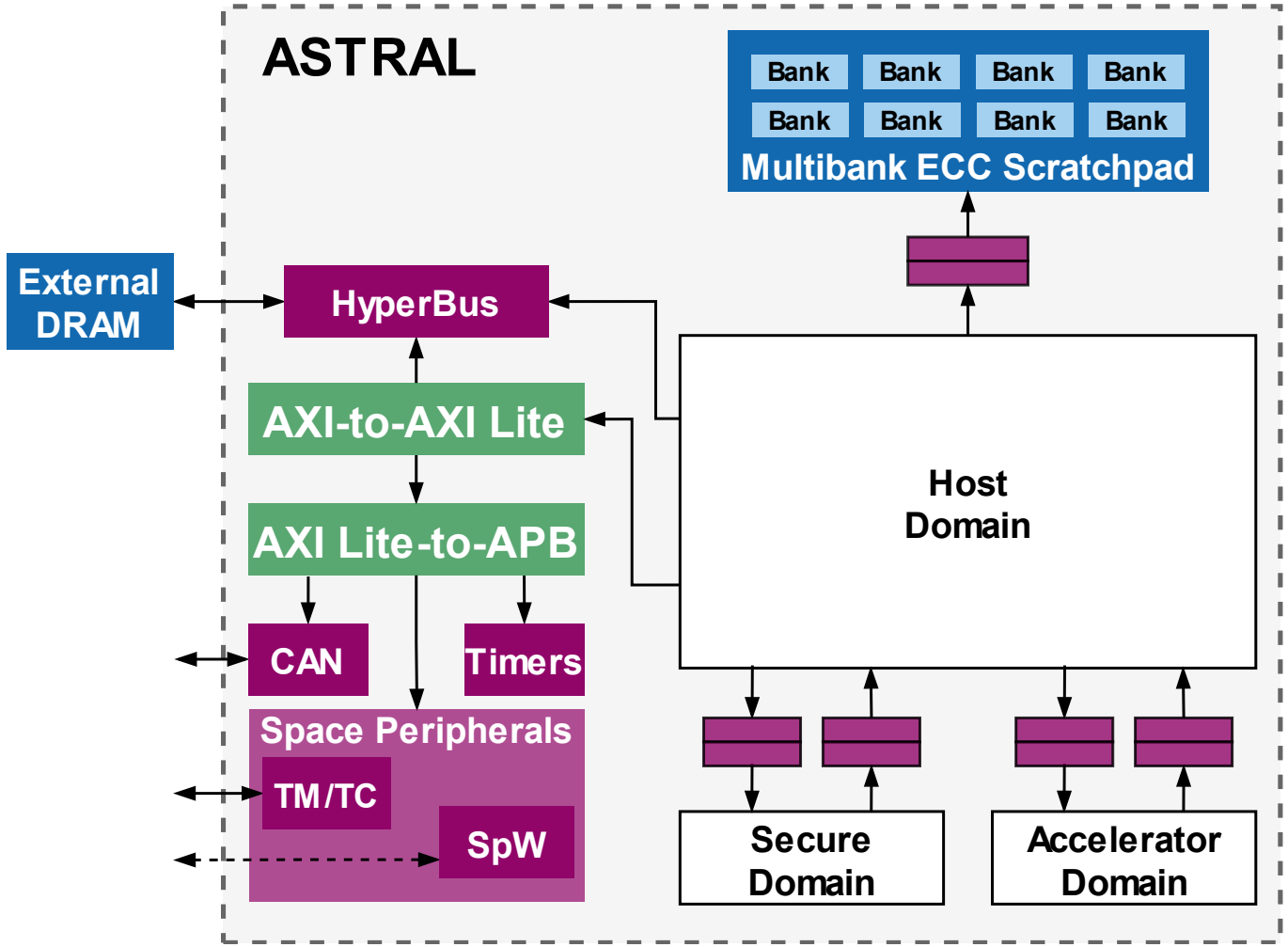
- **FP16 TensorCore** accelerator extended for fault-tolerance for on-chip matrix-multiplication boost
- Transprecision **Integer Neural Engine** for onchip CNN inference acceleration
- **FP16 SoftMax** accelerator for transformers acceleration

ASTRAL SOC - SECURE DOMAIN (OPENTITAN INTEGRATION)



- **OpenTitan**: open-source Root of Trust from lowRISC
- Provides **secure-boot** services verifying the security of the Host domain CVA6 code
- Internal **DMAC**
  - Speed up data transfer during secure boot stage
  - Efficiently serving internal encryption/decryption accelerators
- Refer to OpenTitan docs for more details (https://opentitan.org)

ASTRAL SOC – TAS-I PERIPHERALS INTEGRATION



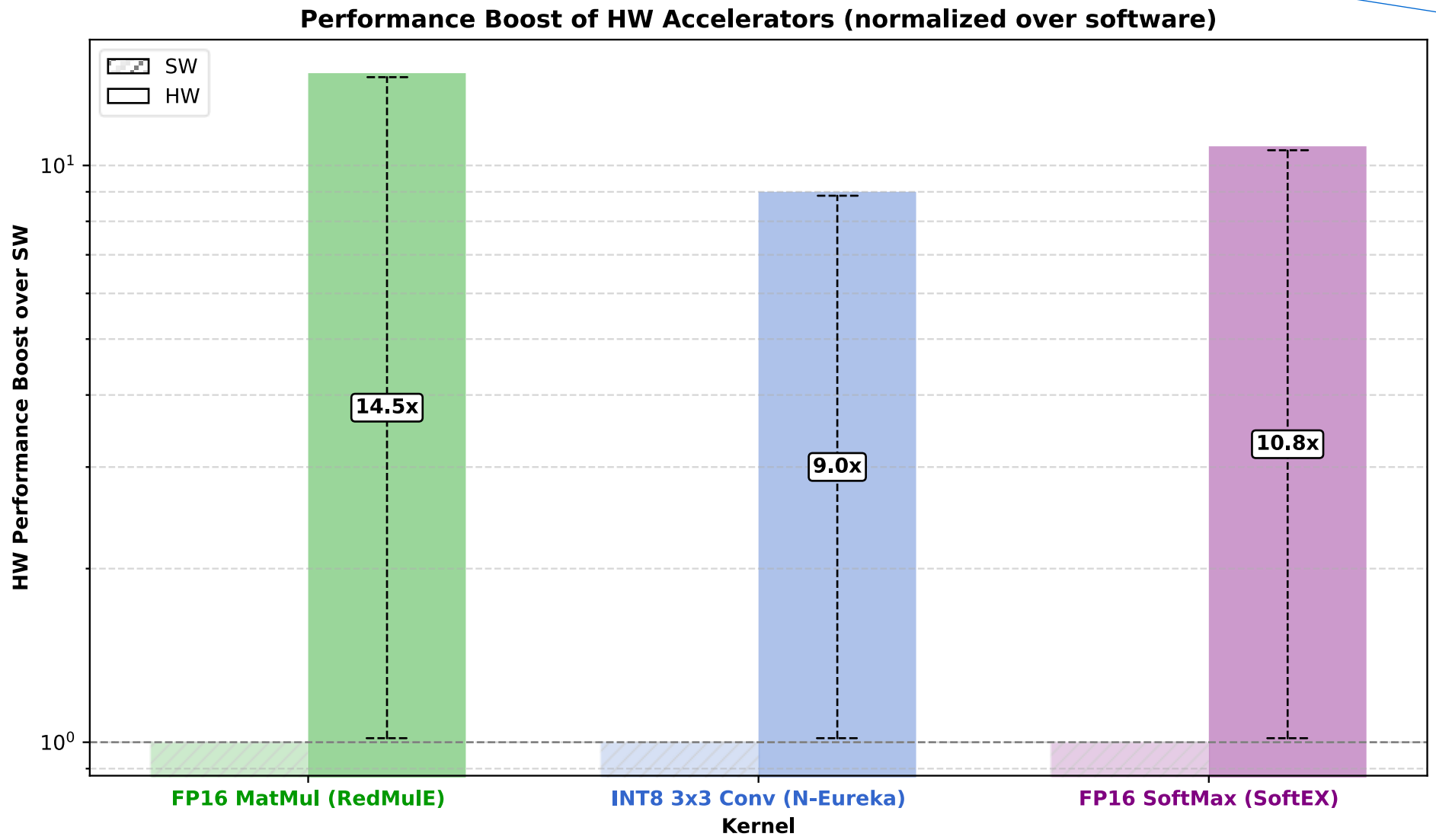
TAS-I proved Astral allows simple integration of proprietary IPs

- **Telemetry** (**TM** - CCSDS 131.0-B-5) and **Telecommand** (**TC** - CCSDS 231.0-B-4) peripheral interface
- **SpaceWire** (ECSS-E-ST-50-12C Rev.1) IP
- IPs libraries easily integrated in the SoC software stack
- Functionally validated through **RTL simulation and FPGA prototyping**

ASTRAL SOC – FPGA IMPLEMENTATION RESULTS

	LUTs	FFs	BRAM	URAM
Astral	**1.23M**	**655114**	**366.5**	**20**
Host Domain	**389841**	**299395**	**276**	**4**
CVA6+L1$+CLIC (x 2)	140102	63135	204 (L1$)	-
Host Memory	59204	33252	64 (L2$)	4 (Scratch.)
IOMMU	6483	5583	-	-
TC/TM	49277	100970	8	-
Spacewire	14088	19680	-	-
Others (Peripherals etc.)	120687	76775	-	-
Secure Domain	**249739**	**146737**	**40**	**16**
Ibex x2	27362	9685	7	-
Crypto Accelerators	83222	47828	13.5	-
Secure Storage	35235	16882	19.5	16
Others (Peripherals ecc.)	103920	72342	-	-
Accelerator Domain	**590537**	**208982**	**50.5**	**-**
RI5CY (x 8)	115400	35384	-	-
DCLS Unit	33554	8305	-	-
TCDM	8243	1152	40	-
HWPEs	351360	98336	-	-
Others	81980	65805	10.5 (I$)	-

ASTRAL SOC – PERFORMANCE RESULTS



ASTRAL - BORN ON THE EARTH, BUILT FOR THE STARS

- Astral is **THE** fully open-source platform for AI in space
- Natively **fault tolerant** -> modular redundancy + ECC and real-time fault recovery (< 100 clock cycles)
- **Parametric** -> straight-forward integration of open-source or proprietary IPs
- **AI acceleration** -> 14.5x and 9x boost on FP/INT AI workloads respect to SW
- **Flexibility** -> Linux OS support with FPGA deployment flow

Thank you!

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Q&A

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Chips-it
FONDAZIONE