10 years of making PULP chips

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Abstract

The Parallel Ultra Low Power (PULP) platform started in April 2013 as a joint effort between ETH Zürich and University of. In the past decade, this project has enjoyed tremendous success and has played a part in the recent emergence of open source hardware as a viable option. For research and commercial development of advanced computing systems more than 50 ASICs were designed and tested related to the PULP Platform. This contribution presents these ASICs and gives an overview of targeted technology nodes and application domains.

Introduction

Open source hardware has made great strides in the past few years. As a member of PULP platform team, I have been very lucky to have taken part in the journey that has resulted in more than 50 ASICs as part of this project. The result of these ASICs have contributed directly to the open source repositories under https://github.com/pulp-platform, and many of the contributions have found new homes with non-for-profit companies and consortia, such as the OpenHW group (RI5CY and Ariane) or LowRISC (Zeroriscy). All these ASICs have been part of the IIS Chip Gallery [1] and with this contribution I would like to present a summary of all the ASICs to commemorate our efforts in open source hardware.

List of PULP related ASICs

The following Table 1 lists the ASICs that were taped-out (or were in planning) at the time of writing.

Table 1: PULP related ASICs

	Year	Name	Technology	Domain
	2013			
1		Pulp	ST28	IoT processing
2		Sir10us	UMC180	IoT control
3		Or10n	UMC180	IoT control
	2014			
4		Artemis	UMC180	IoT processing
5		Diana	UMC180	IoT processing
6		Hecate	UMC180	IoT processing
7		Selene	UMC180	IoT processing
8		Pulpv2	STM28	IoT processing
	2015			
9		Diego	ALP180	IoT control
10		Manny	ALP180	IoT control
11		Sid	ALP180	IoT control
12		Fulmine	UMC65	TinyML, security
13		Mia Wallace	UMC65	IoT processing
14		Pulpv3	ST28	IoT processing
15		VivoSoC	SMIC130	Biomedical
16		Honey Bunny	GF28	IoT processing
17		Imperio	UMC65	IoT control
18		Phoebe	UMC65	IoT control
	2016			
19		VivoSoC2	SMIC130	Biomedical
20		VivoSoC2.1	SMIC130	Biomedical
21		Patronus	UMC65	Security
	2017			
22		Mr. Wolf	TSMC40	IoT / Biomedical
23		GAP8	TSMC55	IoT, Industrial
	2018			
24		Arnold	GF22	Industrial
25		Poseidon	GF22	Processor core
26		Kosmodrom	GF22	Processor core
27		Atomario	UMC65	Processor core
28		Scarabeaus	UMC65	IoT control
29		VivoSoC3	SMIC130	Biomedical
	2019			
30		Baikonur	GF22	HPC, Industrial
31		Billywig	UMC65	Processor core
32		Plink	UMC65	IoT, Industrial
33		Urania	UMC65	Accelerators
34		Xavier	UMC65	Accelerators
35		Rosetta	TSMC65	TinyML
36		VivoSoC3.1	SMIC130	Biomedical
	2020			
37		Dustin	TSMC65	IoT, TinyML
38		Vega	GF22	Industrial
39		Thestral	GF22	Low power
	2021			
40		Darkside	TSMC65	IoT, TinyML
41		Dogeram	TSMC65	Industrial, control
42		Echoes	TSMC65	IoT, TinyML
43		Marsellus	GF22	IoT, TinyML
44		Minpool	TSMC65	HPC
45		Yun	TSMC65	HPC
46		Zest	TSMC65	Industrial, control
47		Kraken	GF22	IoT, TinyML

2022			
48	Cerberus	TSMC65	Safety
49	Eclipse	TSMC65	Processor Core
50	Kairos	TSMC65	Power control
51	Neo	TSMC65	Processor core
52	Trikarenos	TSMC28	Safety
53	Shaheen	GF22	IoT, Industrial
54	Occamy	GF12	HPC
55	Siracusa	TSMC16	AR/VR
2023			
56	Carfield	Intel16	Automotive
57	Iguana	IHP130	Open MPW
58	*tbd*	*TSMC65*	*tbd*
59	*tbd*	*TSMC65*	*tbd*
60	*tbd*	*TSMC65*	*tbd*

Despite the large number of ASICs designing, taping out and testing an ASIC still requires a considerable effort even with the advent of modern design tools and techniques. Practically all of these ASICs were designed from publicly available permissively licensed open source RTL code at the PULP platform GitHub page and mapped onto the technology using a digital design flow. Only technology dependent data (i.e. memories, pads, clock generators, interface IP) were not made available due to non-disclosure agreements, and we hope that in the next decade, open source process design kits and open source design tools will help us have complete, end-to-end PULPdesigns open sourced.

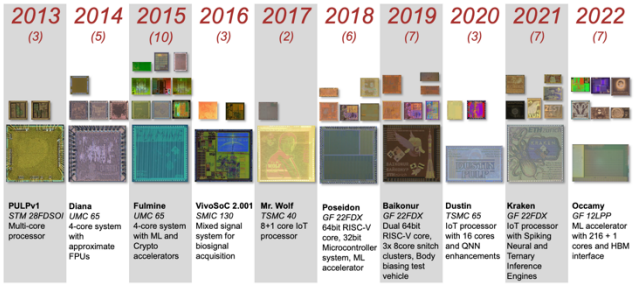

Figure 1 PULP chips by years

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- Our research collaborators, too many to mention within the confines of this paper
- Everyone that has used our open source hardware offerings

We thank you all and hope to present an even more impressive list for the next 10 years.

Short Bios:

Frank K. Gürkaynak, has earned his Ph.D. Degree from ETH Zürich and has been heading the Microelectronics Design Center, of ETH Zürich that supports IC, FPGA and PCB design flows for the university as well as serving as a Senior Scientist in the Digital Circuits and Systems Group. He has worked as part of the PULP platform project since its inception in 2013.

Luca Benini is the chair of Digital Circuits and Systems with ETH Zurich and a full € professor with the University of Bologna. He has served as chief architect for the Platform 2012 in STMicroelectronics, Grenoble. His research interests include energy-efficient systems and multicore SoC design. He is also active in the area of energy-efficient smart sensors and sensor networks. He is a fellow of the ACM, IEEE and a member of the Academia Europaea.

References

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