On-Demand Redundancy Grouping (ODRG)

Selectable Soft-Error Tolerance for a Multicore Cluster

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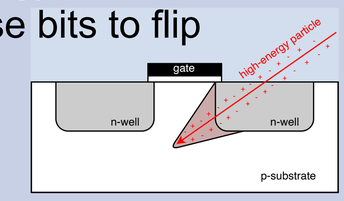
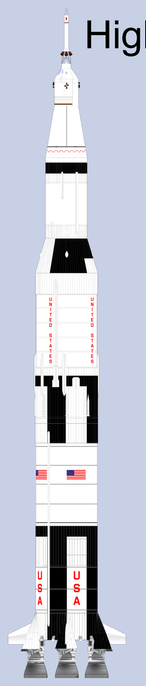
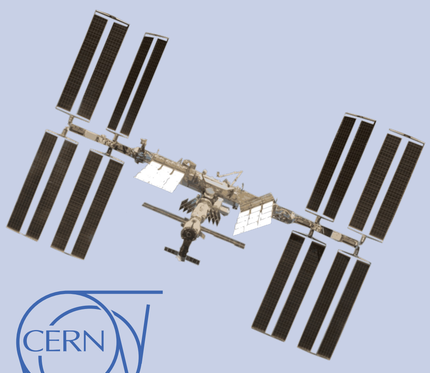
ETH zürich

Radiation in Space

High-energy particles can cause bits to flip







CERN

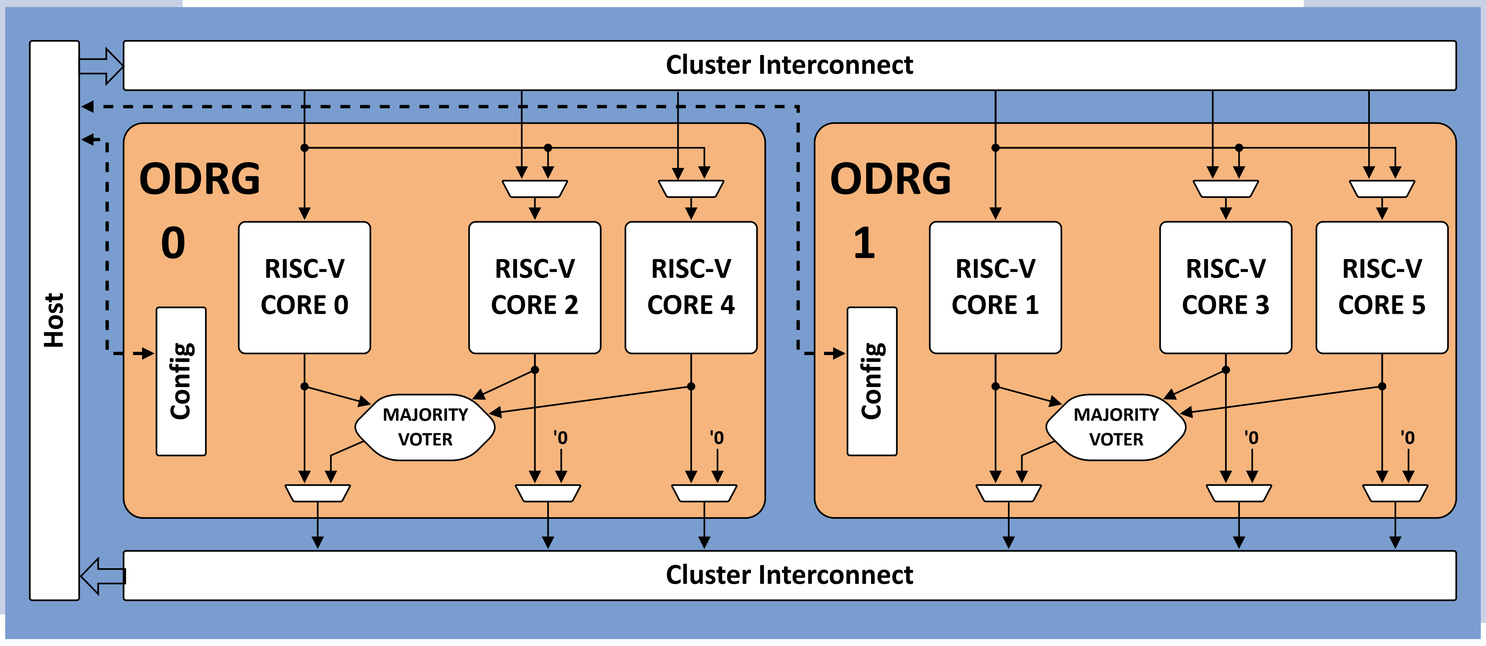
State-of-the-Art Mitigation

- Double/Triple Modular Redundancy (DMR/TMR)
- ARM TCLS [1]
- Software Redundancy

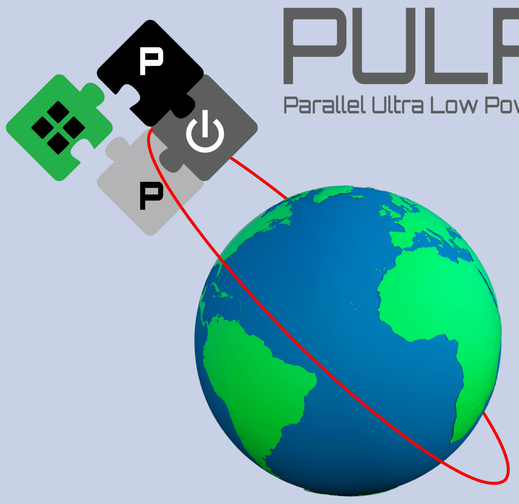
We present a RISC-V multicore cluster that leverages the tradeoff between redundancy mechanisms and performance.

ODRG is an augmentation to open-source RISC-V clusters, allowing a six-core cluster to operate as **two fault-tolerant cores or six individual cores** for high performance, with limited overhead to switch between these modes at run-time.

Our Approach: ODRG

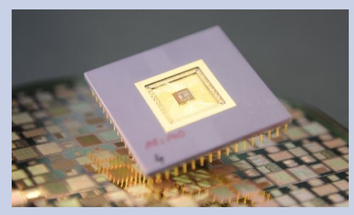


PULP
Parallel Ultra Low Power



lowRISC

RISC-V



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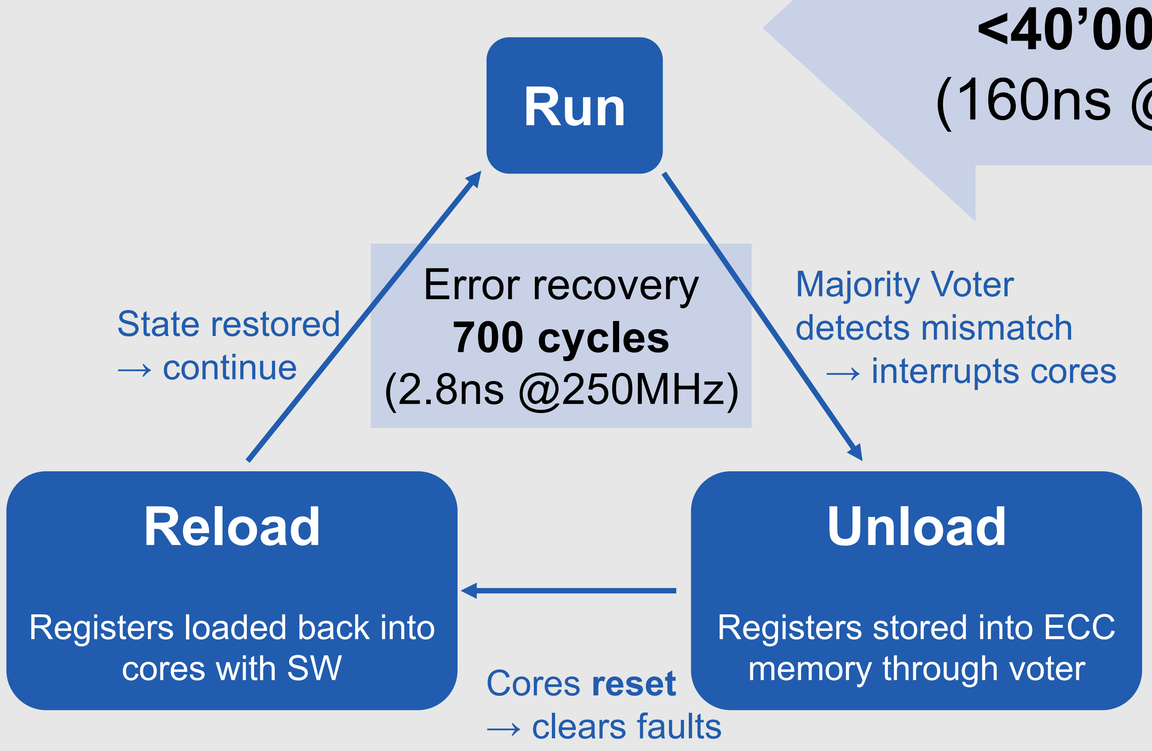
Soft-Error Tolerant Mode

2-core cluster with full fault tolerance

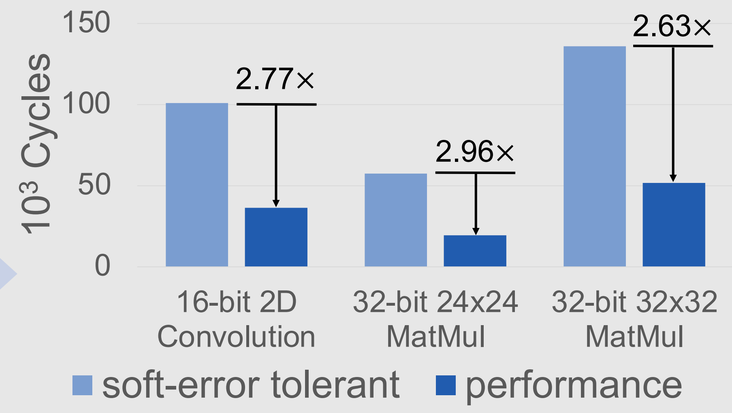
- All cores receive identical inputs
- All outputs are majority voted
- Mismatch triggers **re-synchronization**



Switching requires
<40’000 cycles
(160ns @250MHz)

Performance Mode

6-core cluster for high performance



2.96× speedup
for non-redundant applications

Tasks with >60’000 cycles benefit

Try it out on pulp-platform github!
github.com/pulp-platform/redundancy_cells

References:
[1] X. Iturbe et al., “The Arm Triple Core Lock-Step (TCLS) Processor,” ACM Transactions on Computer Systems, vol. 36, no. 3, pp. 1–30, Aug. 2019.

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