ETH zürich

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

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TECHNOSAPIENS FOR SAVING HUMANITY

Trikarenos

A Fault-Tolerant RISC-V-based Microcontroller for CubeSats in 28nm

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PULP Platform
Open Source Hardware, the way it should be!

@pulp_platform
pulp-platform.org
youtube.com/pulp_platform

CubeSats & Micro Satellites

- Small satellites becoming more popular
- Very low power envelope
- Increasing processing requirements
- Existing space-ready processors based on old technologies

Source:https://www.esa.int/var/esa/storage/images/esa_multimedia/images/2016/04/cubesats_orbiting_earth/15950521-1-eng-GB/CubeSats_orbiting_Earth.jpg

Leverage modern, open-source Microcontroller SoC!

Open-Source Microcontroller – PULPissimo

pulp-platform / **pulpissimo** Public

This is the top-level project for the PULPissimo Platform. It instantiates a PULPissimo open-source system with a PULP SoC domain, but no cluster.

View license

294 stars 136 forks

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bluewww Merge pull request #350 from pulp-platform/x-in-bootrom ... on Nov 3, 2022 694

View code

README.md

PULPissimo

README.md

PULPissimo

Citing

If you are using the PULPissimo IPs for an academic publication, please cite the following paper:

```
@INPROCEEDINGS{8640145,
  author={Schiavone, Pasquale Davide and Rossi, Davide and Pullini, Antonio and
  booktitle={2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified C
  title={Quentin: an Ultra-Low-Power PULPissimo SoC in 22nm FDX},
  year={2018},
  volume={},
  number={},
  pages={1-3},
  doi={10.1109/S3S.2018.8640145}}
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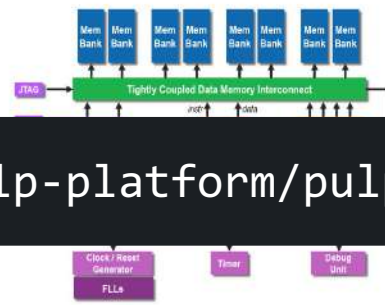
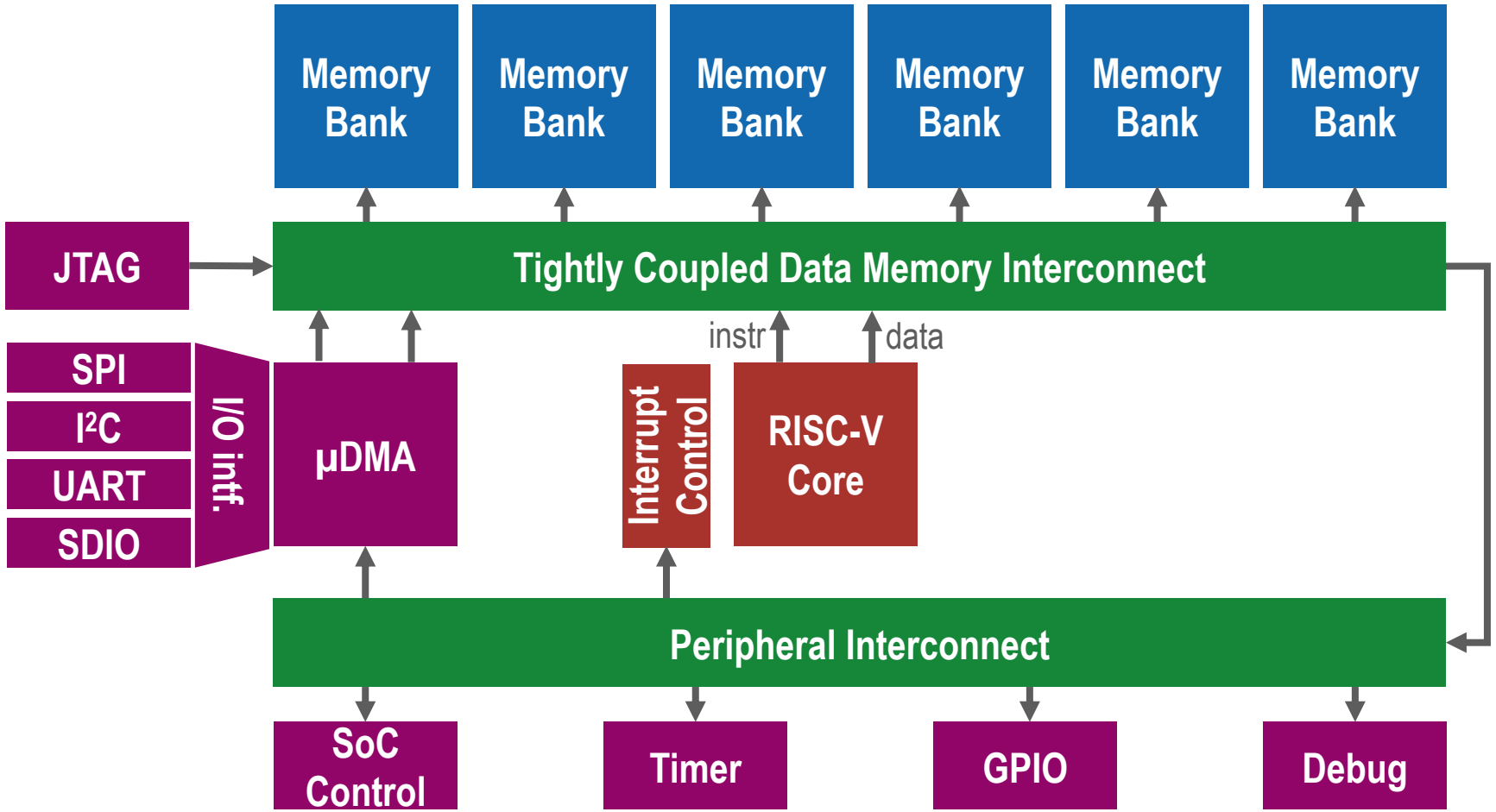


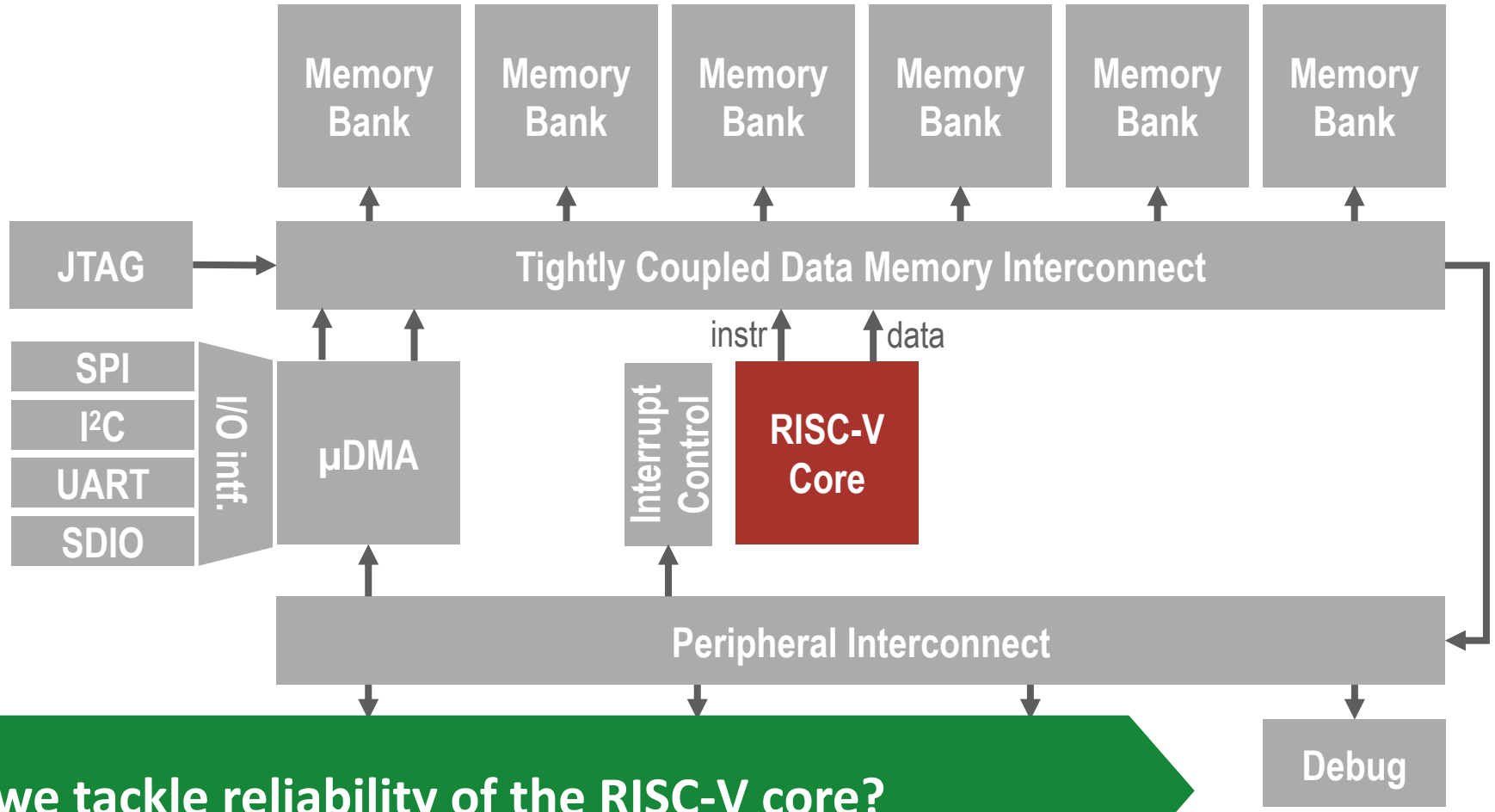
PULPissimo is the microcontroller architecture of the more recent PULP chips, part of the ongoing "PULP platform" collaboration between ETH Zurich and the University of Bologna - started in 2013.

github.com/pulp-platform/pulpissimo

PULPissimo Architecture

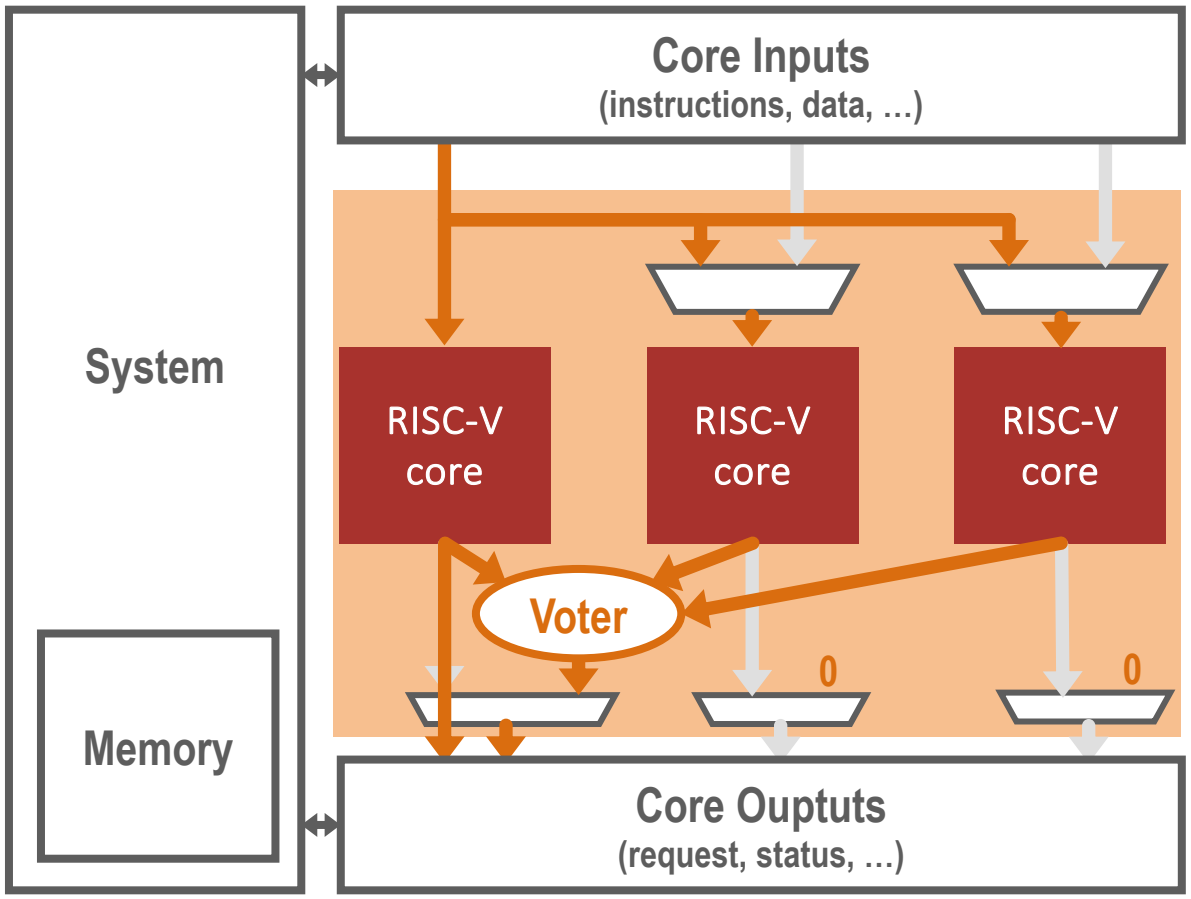


PULPissimo Architecture



How do we tackle reliability of the RISC-V core?

Reliable Processing Cores

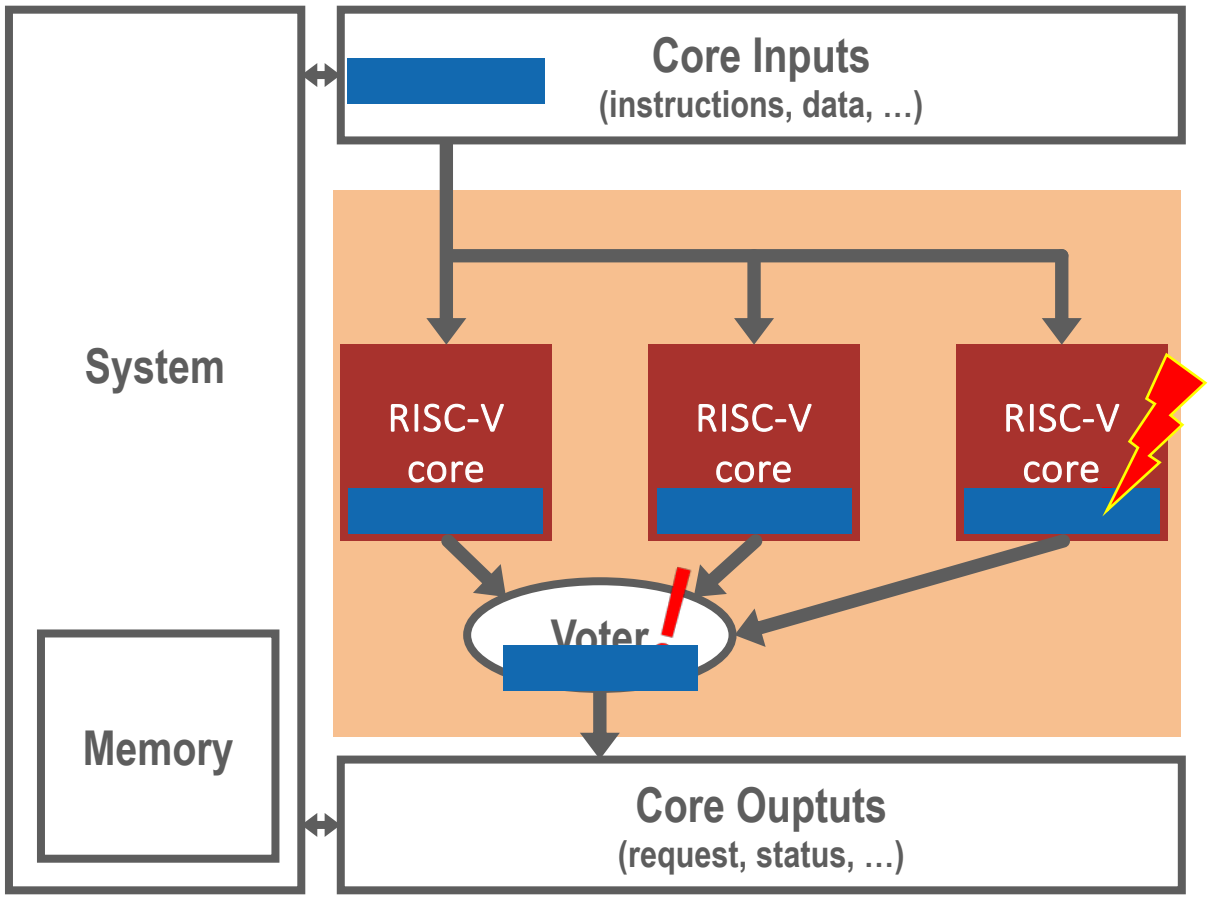


- Replicate Core

  →Triple-Core Lockstep

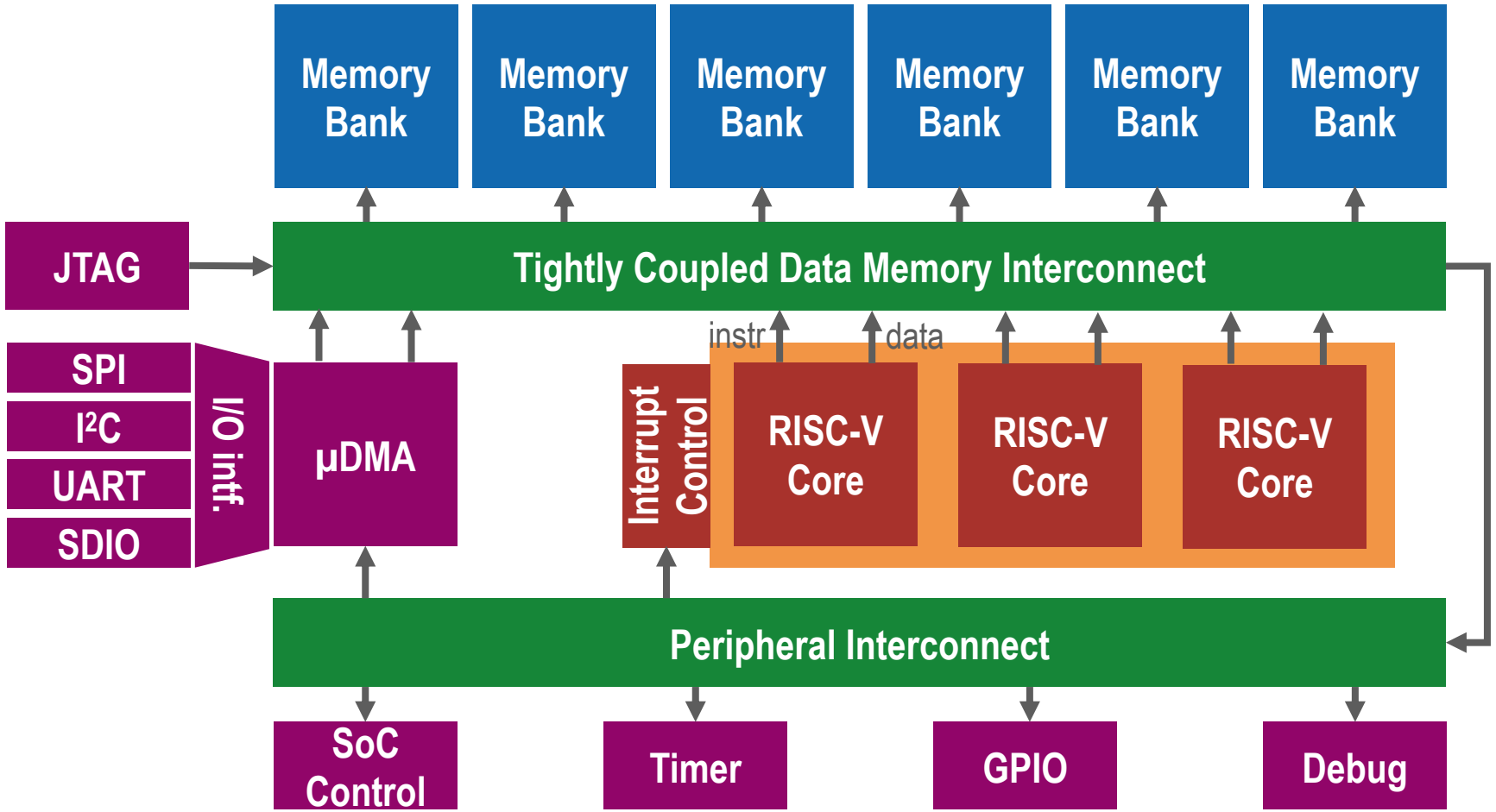
- Identical Inputs
- Voted Outputs
  - Directly connects any soft error
- Configurable for performance if reliability is not needed
  - **2.96x speedup**

Software Recovery of Triple Modular Redundant Cores

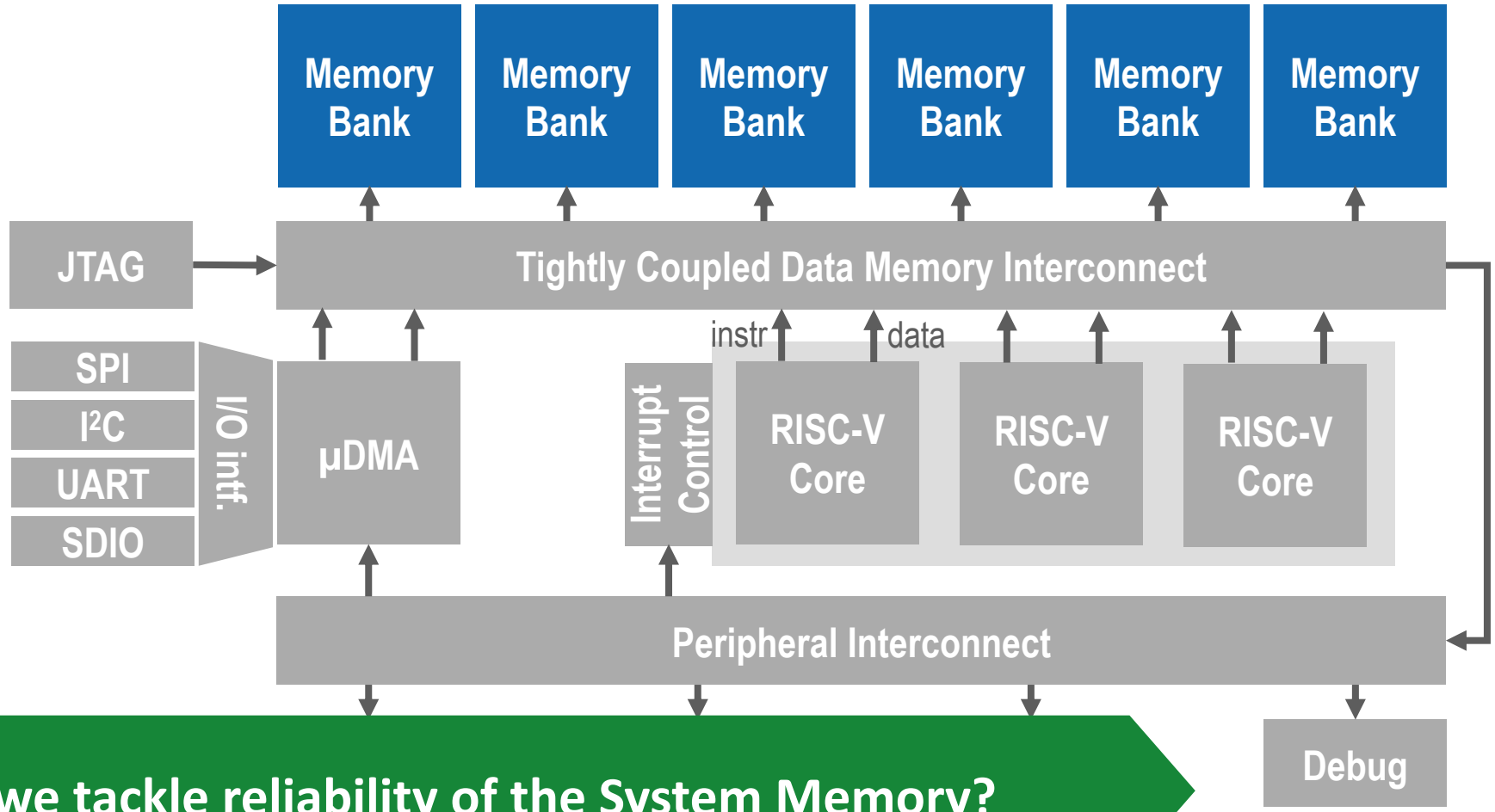


- Radiation causes soft-error
- Error detected by voter
- Core state (RF, PC, CSRs) stored to memory
  - Corrected by voter
- Core state loaded back into cores
- Total procedure in ~600 cycles

Trikarenos – PULPissimo with Reliability

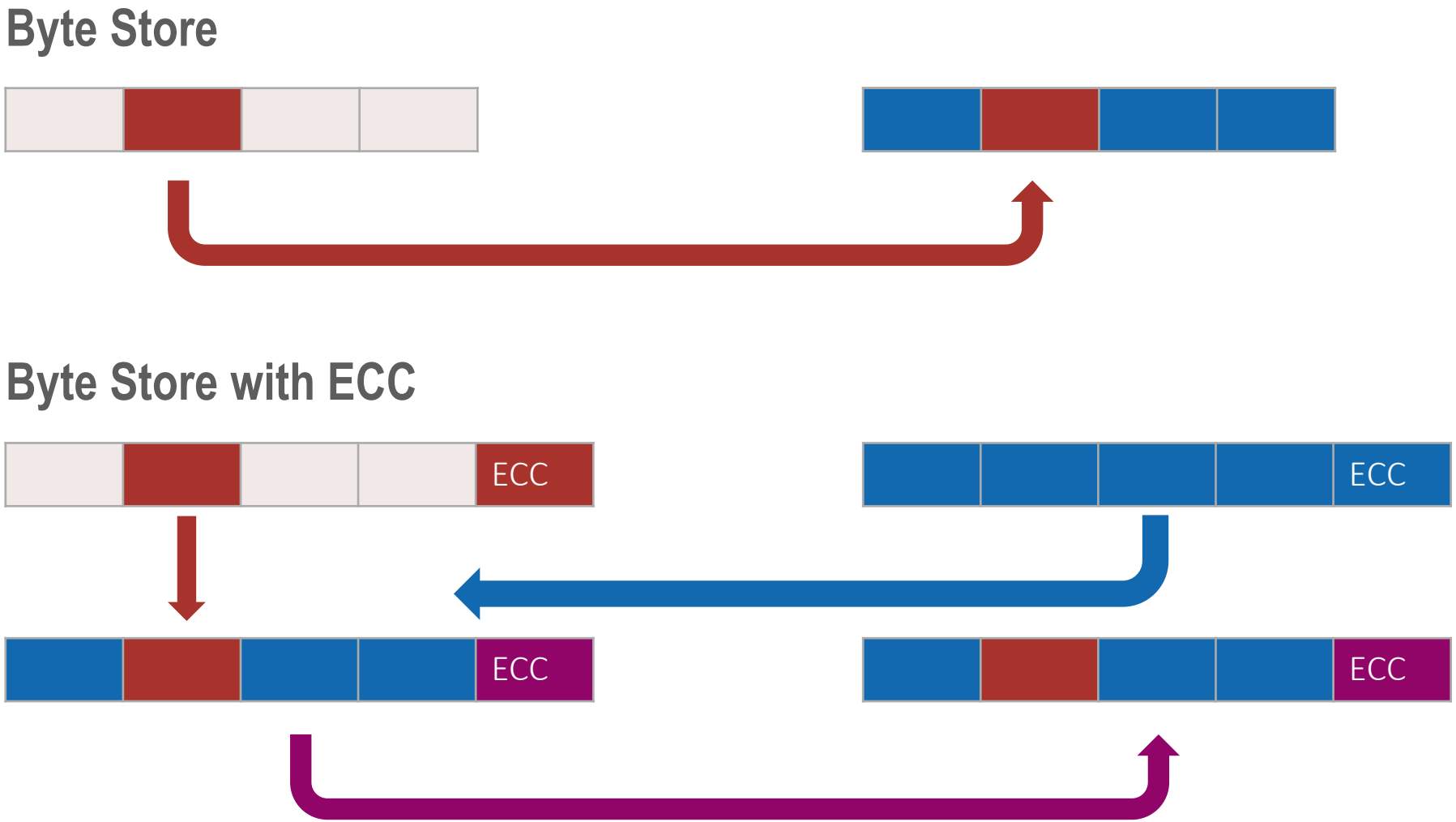


Trikarenos – PULPissimo with Reliability

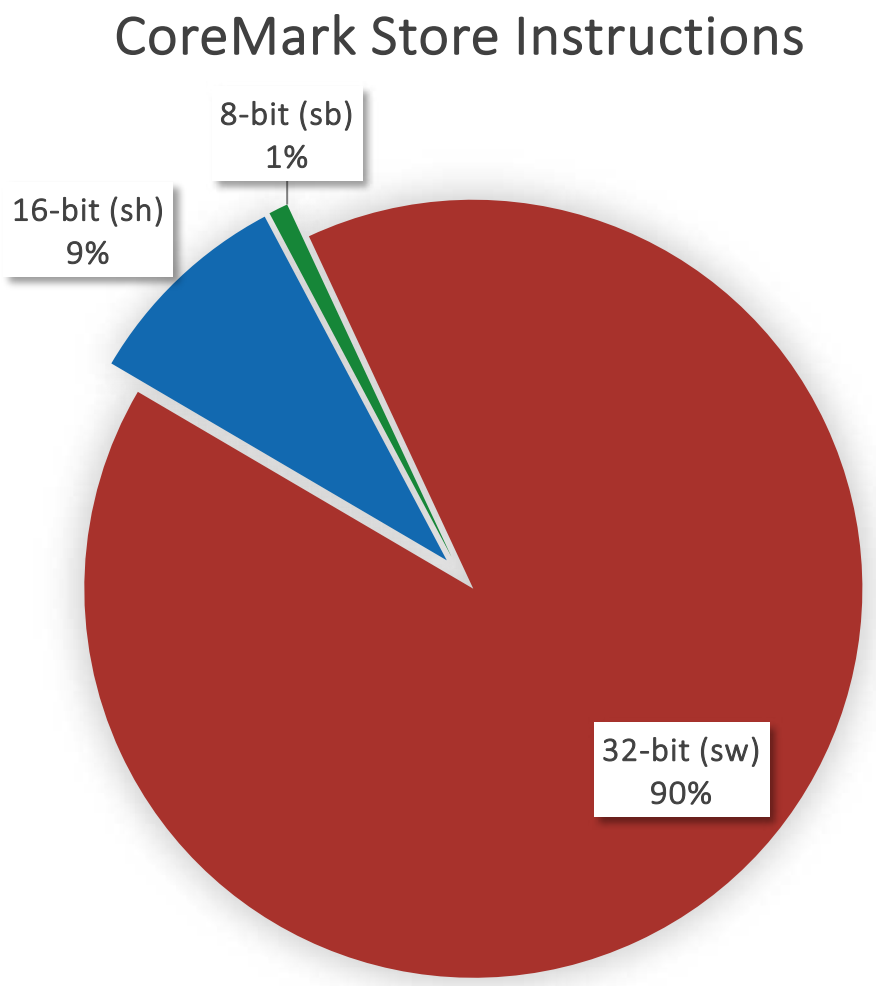


How do we tackle reliability of the System Memory?

Byte-addressable Memory – ECC Load and Store

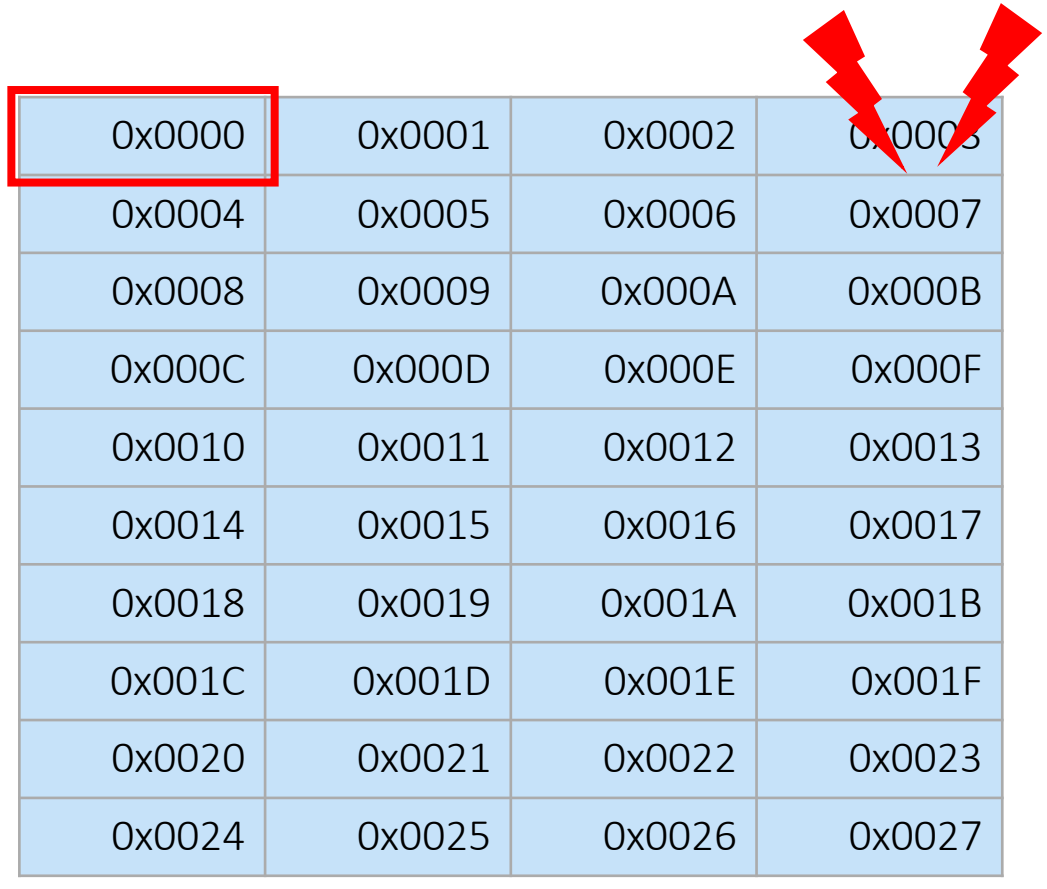


ECC Load-and-Store – Performance Impact



- 32-bit Hsiao ECC word protection
- Directly grant storage
  - Delay following transaction, not current transaction, to shift & reduce impact
- Results: **<1% cycle increase**
  - Various tests, such as 8-bit Matrix-Matrix Multiplication

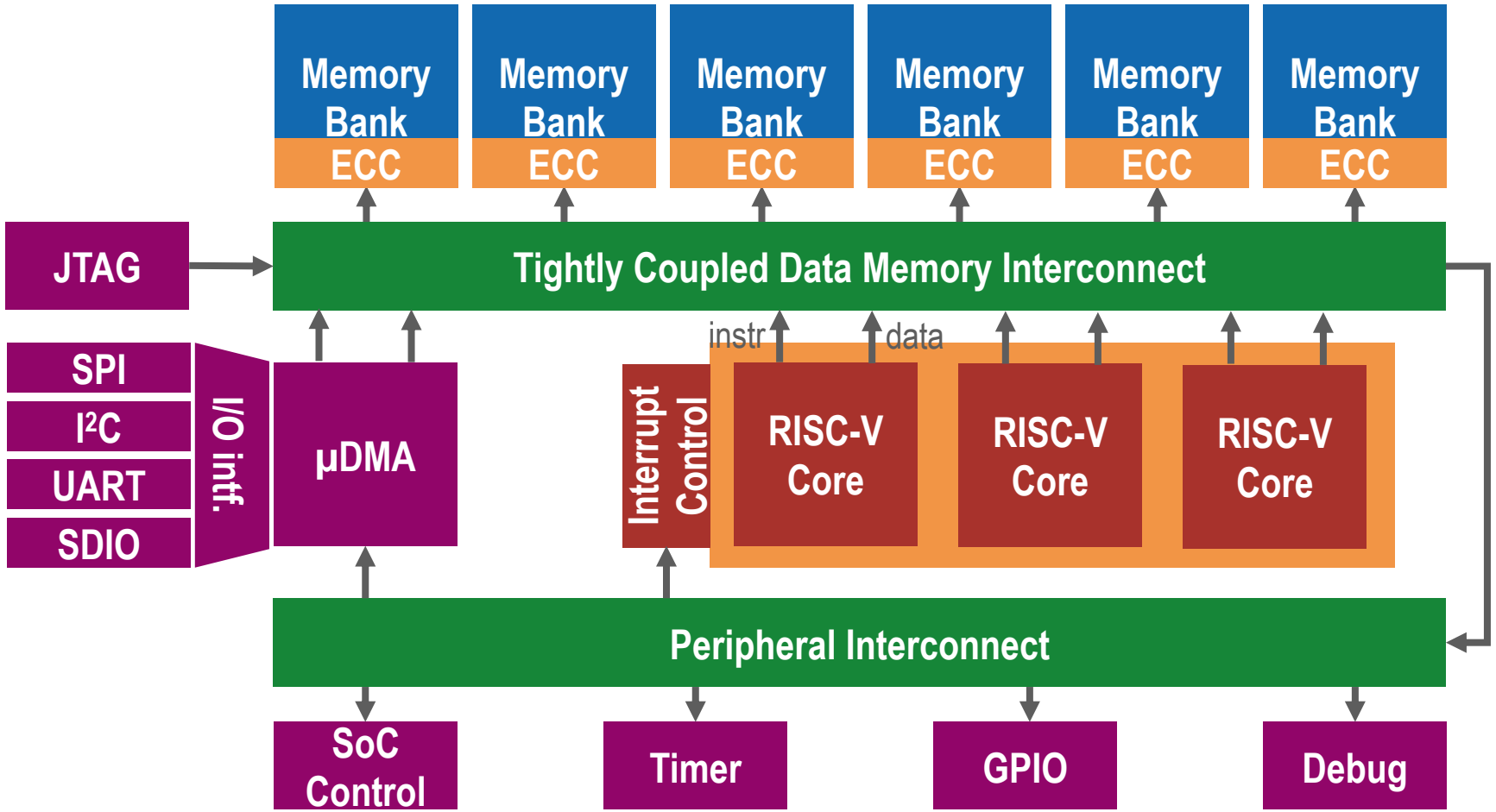
ECC Scrubber



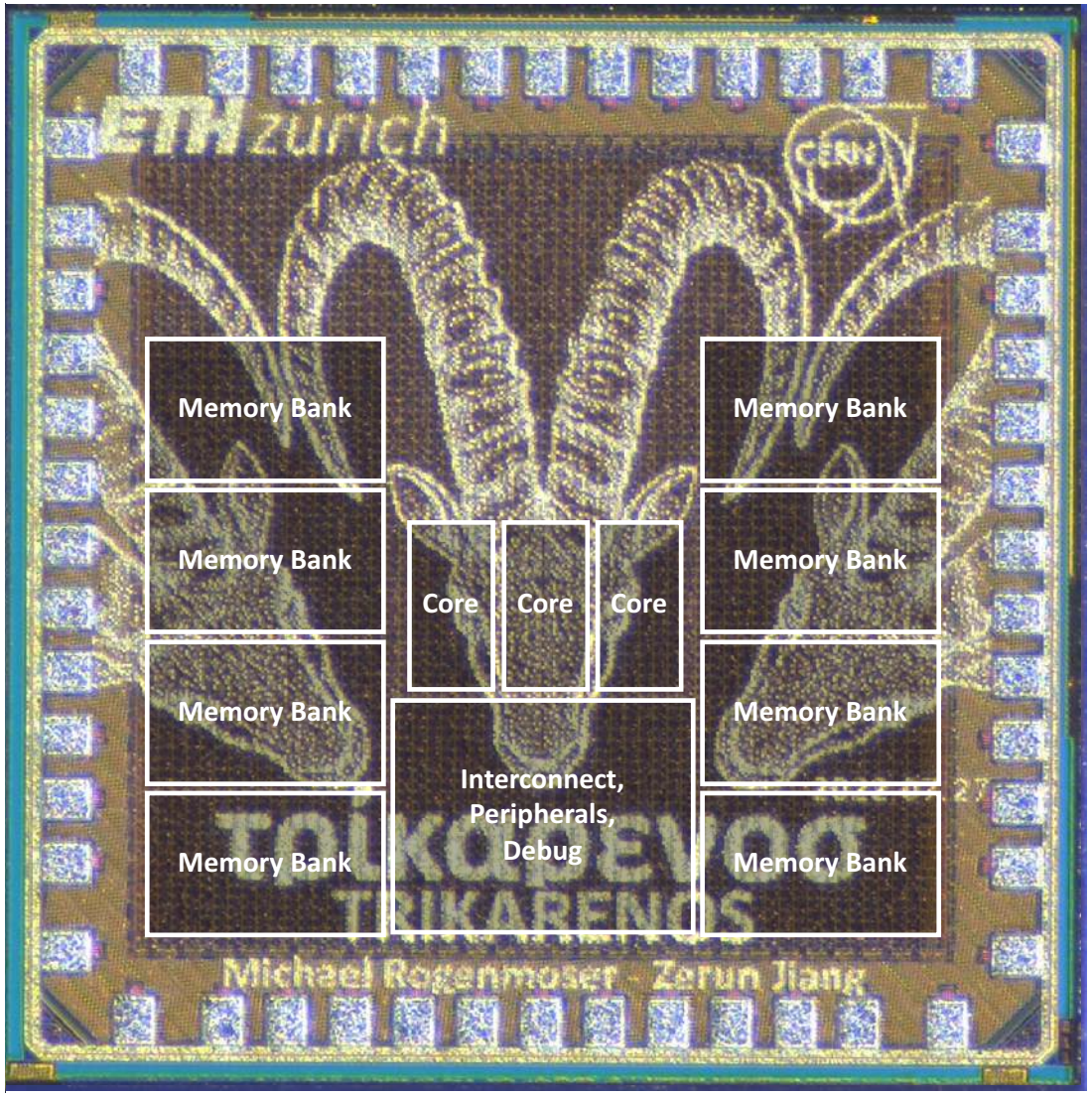
0x0000	0x0001	0x0002	0x0003
0x0004	0x0005	0x0006	0x0007
0x0008	0x0009	0x000A	0x000B
0x000C	0x000D	0x000E	0x000F
0x0010	0x0011	0x0012	0x0013
0x0014	0x0015	0x0016	0x0017
0x0018	0x0019	0x001A	0x001B
0x001C	0x001D	0x001E	0x001F
0x0020	0x0021	0x0022	0x0023
0x0024	0x0025	0x0026	0x0027

- Multiple errors in a single word lead to unrecoverable errors
- Scan Memory Bank
- Re-write faulty word if error is detected
- Defer permission to external accesses
- Log all corrections (and uncorrectable words)

Trikarenos – PULPissimo with Reliability



Trikarenos – ASIC implementation

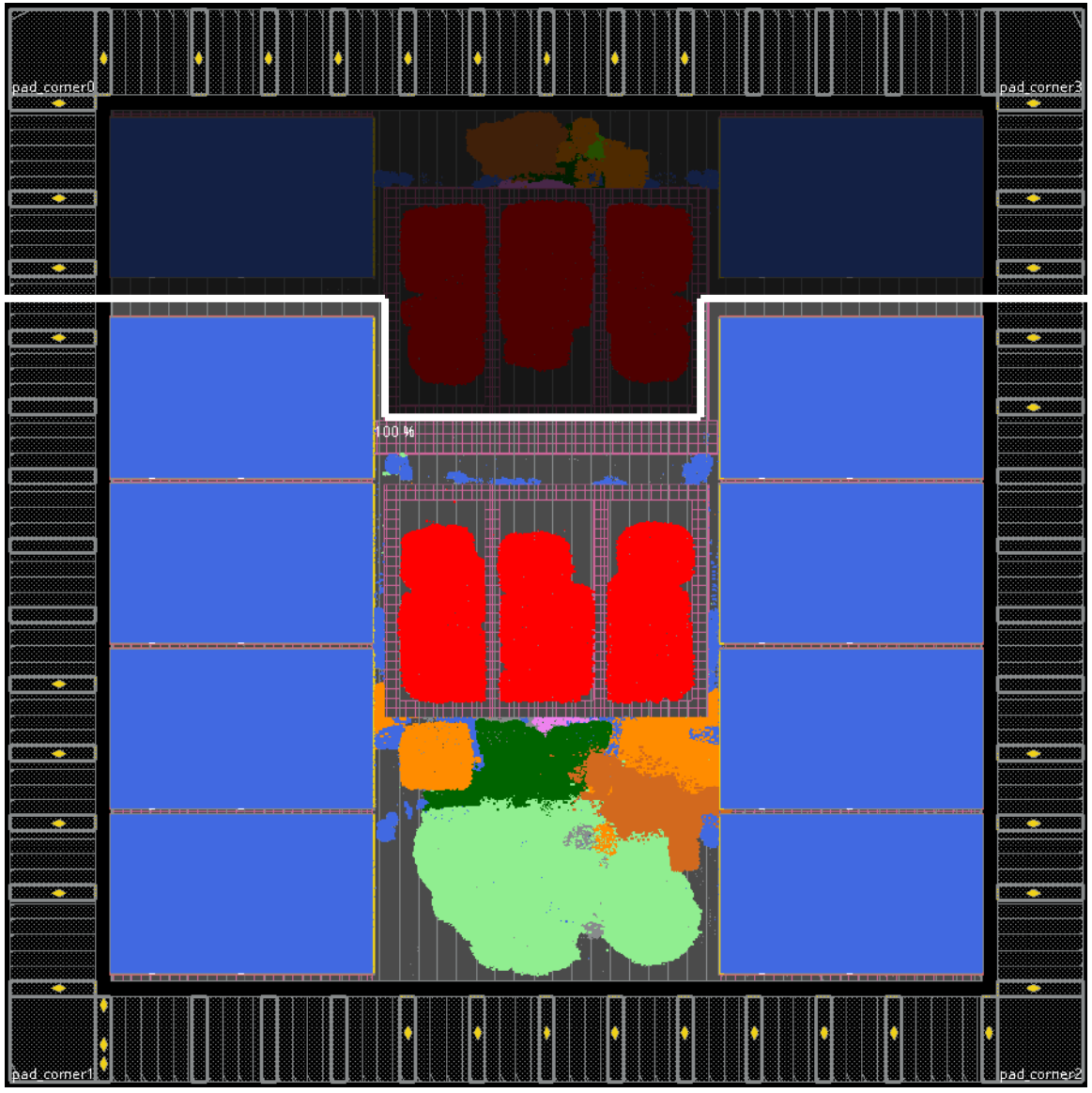


- TSMC 28HPC+
  - Shown to have high TID tolerance
- 2 mm^2 @250 MHz
- 3 separate Ibex cores
- 256 KiB Memory in 8 word-interleaved banks

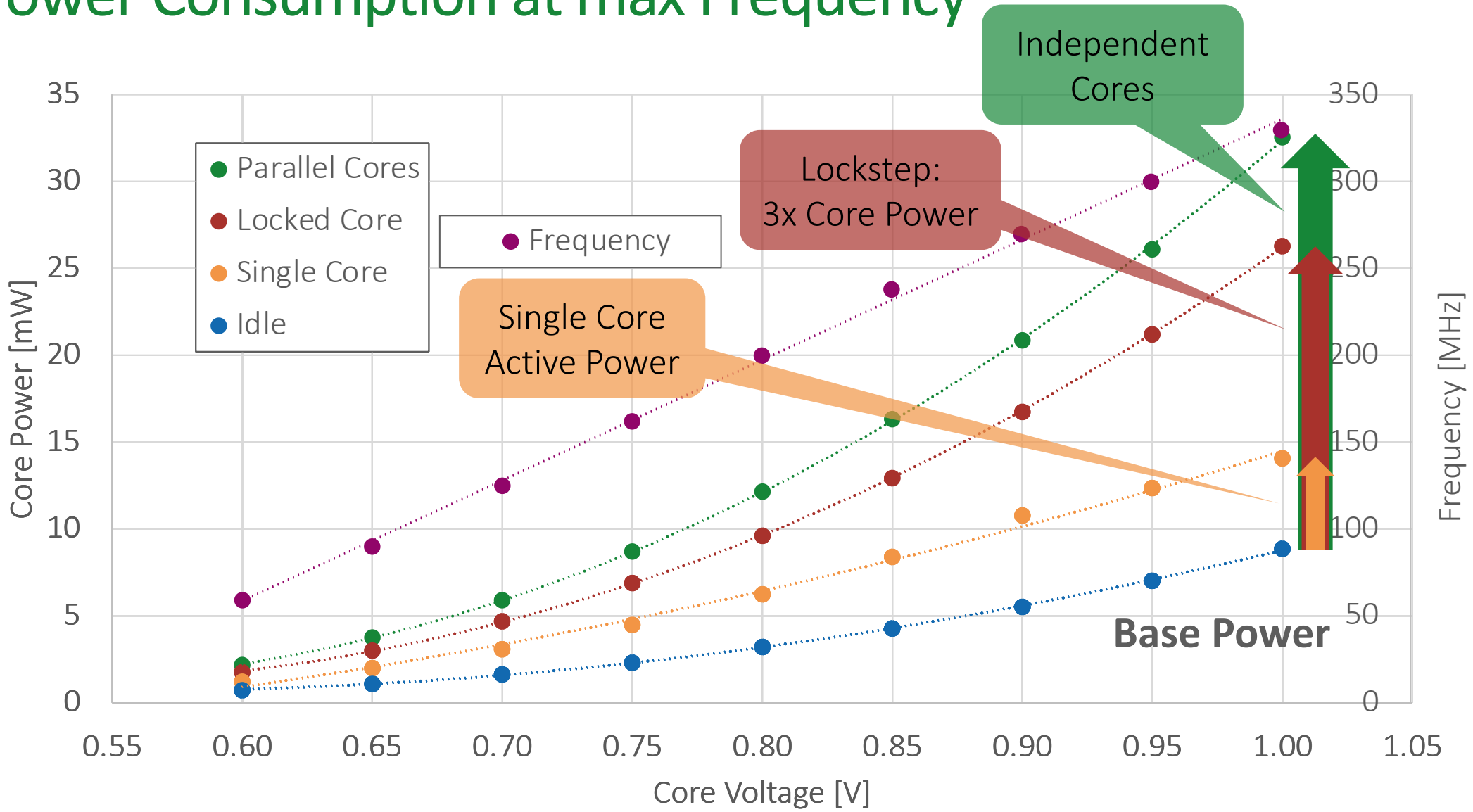
Internal structure

- Spatially separated cores with a keepout zone

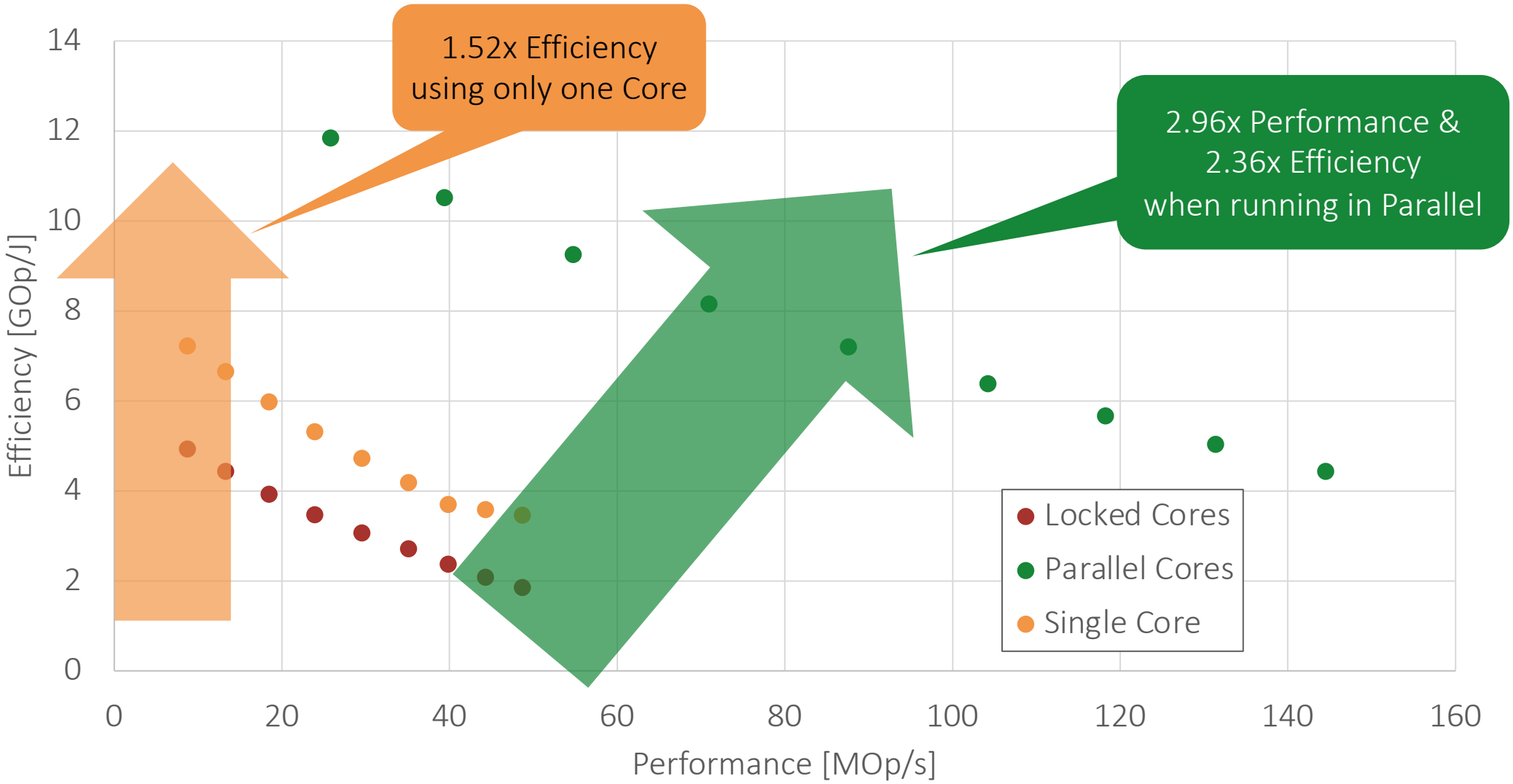
- Legend:
  - Cores
  - HMR Unit
  - Memory (w/ ECC en-/decode)
  - Interconnect
  - Debugger
  - Logging & control registers, ROM, …
  - I/O



Power Consumption at max Frequency



Efficiency vs. Performance



How do we compare?

	RAD750[9]	GR716[11]		C[10]	**Trikarenos**
Number of Cores	1	1		1	**1(3)/3**
Instruction Set Architecture	Power	SPARC		RISC	**RISC-V**
Technology	0.250µm			28nm	**28nm**

2.6x reliable Performance vs. GR716

Configurable Core Configuration => 3x core count

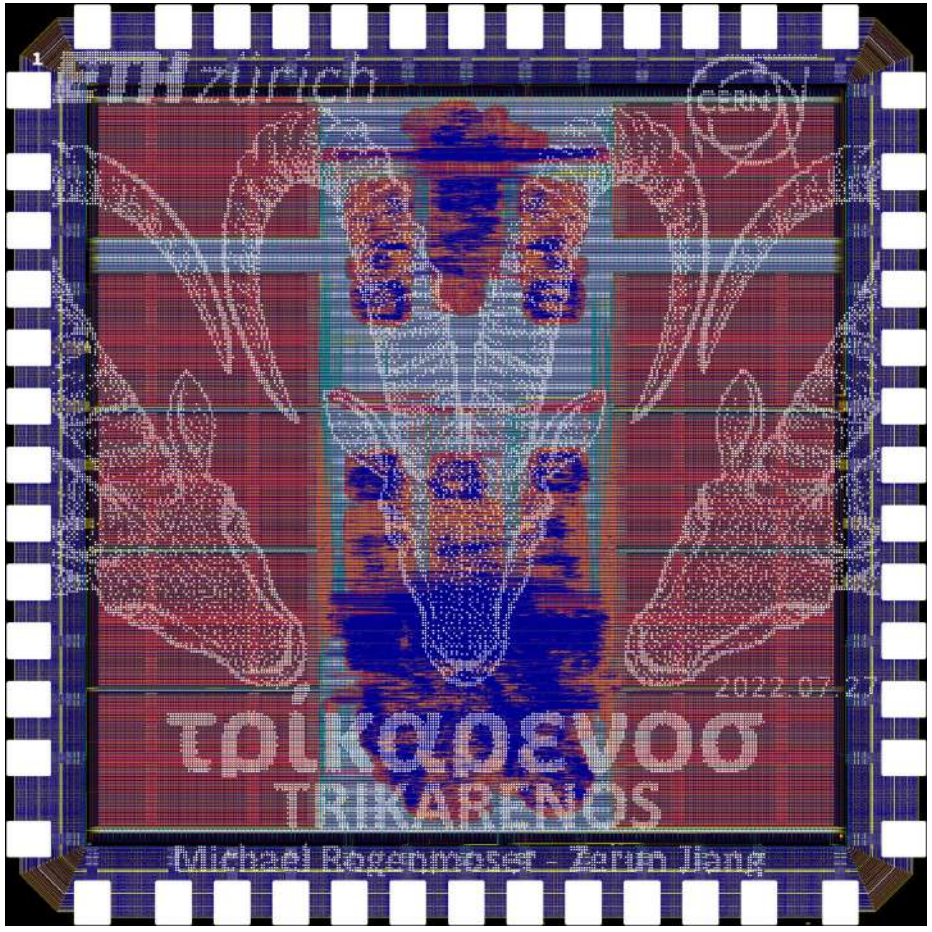
Configuration Switching => 2.96x Performance

63x Efficiency vs. GR716

21.5x (50x) Efficiency vs. ARM TCLS

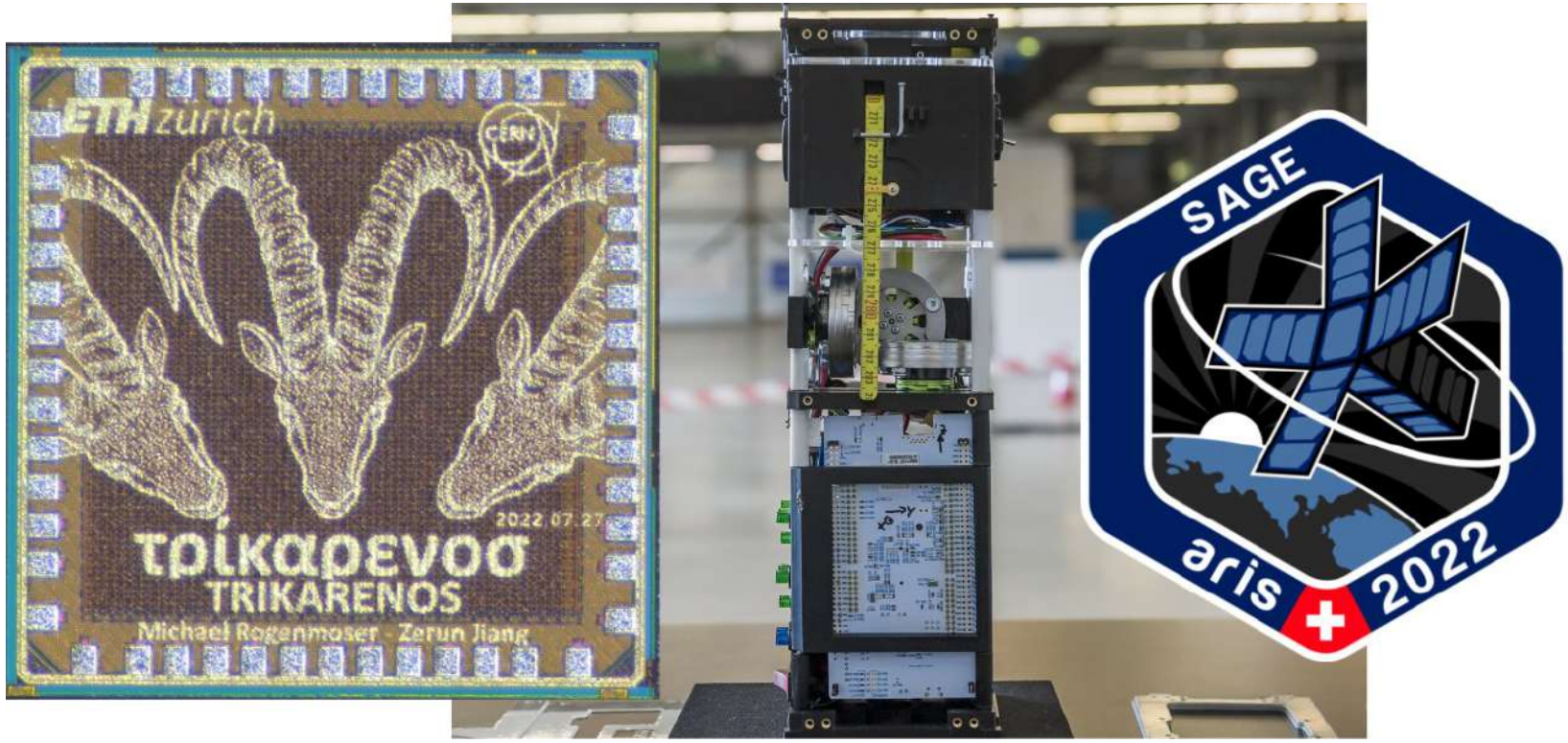
Conclusion

- Trikarenos: Efficient, Fault-Tolerant Microcontroller
  - Configurable Triple-Core Lockstep
  - 256 KiB low-latency ECC-protected Memory
  - Peripheral DMA
- Implemented in 28nm
  - Up to 330 MHz @ 32.5 mW
- Runtime Configurable
  - Reliable when needed
  - Performant when possible



Outlook – Radiation tests & SAGE CubeSat

- Currently ongoing: Functional test under radiation
- Future: Integration into demonstration CubeSat



PULP

Parallel Ultra Low Power

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all our past collaborators and many more that we forgot to mention

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