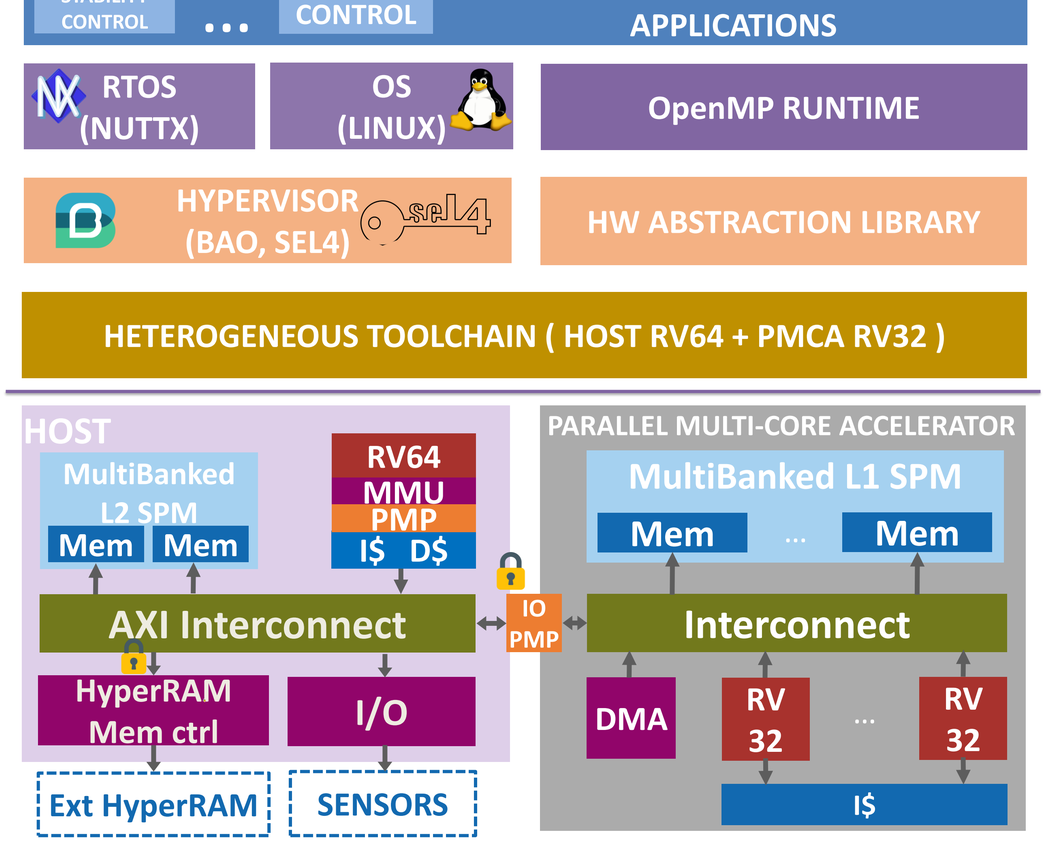
Shaheen: An Open, Secure, and Scalable RV64 SoC for Autonomous Nano-UAVs

- **Versatility & safety:** nano drones are small and agile, making them ideal for accessing hard-to-reach areas or tight spaces and performing inspection & maintenance.
- **Cost-effectiveness:** nano drones are relatively inexpensive to produce and operate.

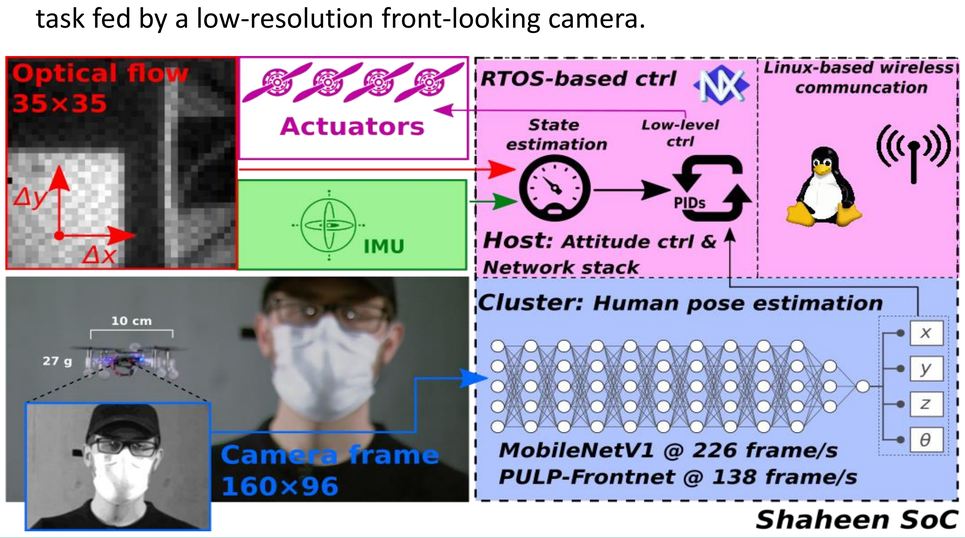
- **Software stack and energy efficiency:** as they evolve from research prototypes to products, their flight computers need to: (i) run increasingly complex multi-tasking workloads with large memory footprints within a **few hundred mW power budget**; (ii) support **virtualization and secure operation** in uncontrolled or even hostile deployment scenarios.

Shaheen addresses these challenges, ensuring ***Performance*** while maintaining ***Energy Efficiency*** and providing ***advanced virtualization support***. The design incorporates an ***energy-efficient Programmable Multi-Core Accelerator*** for neural network inference and a Host Subsystem based on ***CVA6***, a 64-bit Linux Capable CPU, enhanced with ***Hypervisor support*** and a lightweight mechanism ***for timing-channels mitigation*** to isolate concurrent execution of multiple software stacks (trusted and untrusted), preventing security threats and ensuring multi-domain operations.

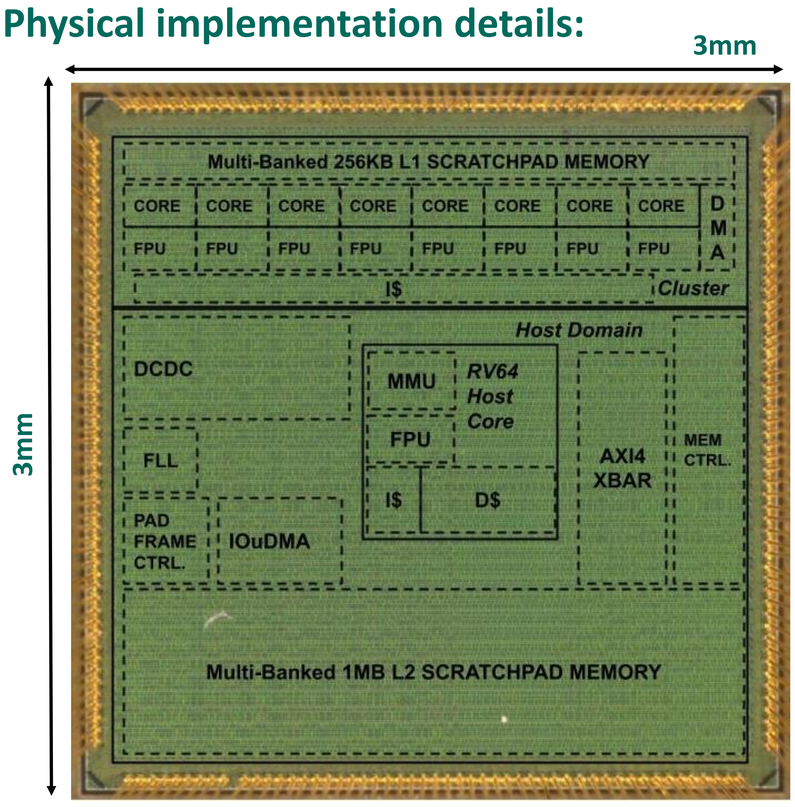
HW-SW stack & Application scenario:



- **HW-SW stack:** The Host core is, to the best of our knowledge, the first silicon implementation fully compliant with the ratified RISC-V ISA hypervisor extension, ensuring multi-domain operations.
- **Application scenario:** the Host processor fuses sensor data to implement real-time attitude control and runs Linux-based legacy software such as wireless network stack. The PMCA runs the CNN-based pose estimation task fed by a low-resolution front-looking camera.

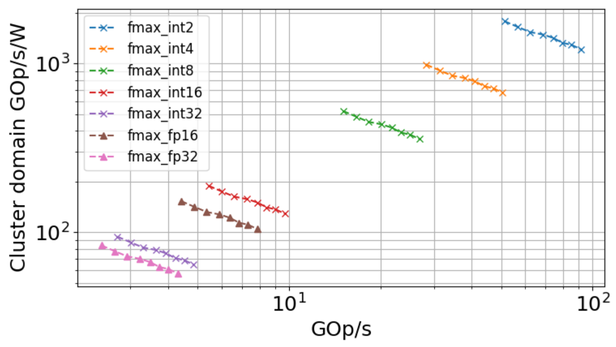


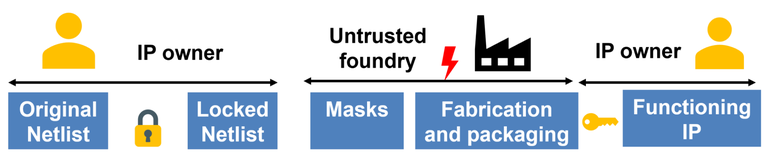
Physical implementation details:



L2 mem., L1 mem (SRAM)	1MiB, 256KiB
Off-chip CPU mem. (HyperRAM)	8MiB - 512MiB
VDD Range	0.625-0.8V
Cluster Max Freq. , CVA6 Max. Freq.	500MHz, 600MHz
Power Envelope	200mW

- **Memory hierarchy:** Nano-UAVs' State-of-the-Art (SoA) SoCs rely on 32-bit processors, small on-chip SPMs and off-chip memories accessible through peripheral interfaces. Instead, Shaheen's memory hierarchy features a 1MB SPM and an ultra-low-power, low-area, low-pin-count, fully-digital HyperRAM memory controller that can drive up to 512MB @1.6Gbps directly on the AXI-4 bus.
- **PMCA energy-efficiency:** The PMCA is built around 8 Ri5cy (RV32) cores sharing 16 16kB SRAM banks. The cores feature dedicated RV32 extension, including hardware loops, post-increment LD/ST, unified MAC&Load operation, narrow bit-width, and mixed-precision SIMD extensions (down to 2-bit) relevant for inference of quantized neural networks. The PMCA's cores also feature FPUs supporting FP32, SIMD FP16, and bfloat.





- **Logic Locking:** Shaheen integrates logic locking, which consists in modifying a hardware IP to add a new input, specifically a logic locking key, to be applied to unlock the original IP functionality. Without the proper logic locking key loaded, the chip is non-functional.

	STM32-H7	STM32-F4	GAP8	Vega	Kraken	Shaheen
Target board	Pixhawk	Crazyflie	AIDeck	AIDeck	AIDeck	**AIDeck / Pixhawk**
Technology	40nm	90nm	55nm	22nm FDSOI	22nm FDSOI	**22nm FDSOI**
Die Size	-	-	10mm2	12mm2	9mm2	**9mm2**
CPU	Cortex M7	Cortex M4	9x RI5CY	10x RI5CY-NN	9x RI5CY-XNN	**CVA6 + 8x FLEX-V**
Supported OS	RTOS	RTOS	RTOS	RTOS	RTOS	**Linux/RTOS/Hypervisor**
Host-compute FP support	SP-FPU, DP-FPU	-	-	SP-FPU	SP-FPU	**SP-FPU, DP-FPU**
Security Features	Crypto/hash accelerators	-	-	-	-	**Side-channel protection, Logic Locking, IOPMP**
Peak SW Performance	240MFOp/s(FP32) 390MOp/s (8b)	72MOp/s (8b)	6 GOp/s (8b)	7GFOp/s(FP16) 15,6GOp/s(8b)	3,12GFLOPs(FP32) 85GOp/s(2b)	**7.9GFOp/s(FP16) 90 GOp/s(2b)**

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