DATE 26
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PALAZZO DELLA GRAN GUARDIA

Democratizing Silicon:
The Rise of Open-Source EDA and Europe's Strategic Roadmap

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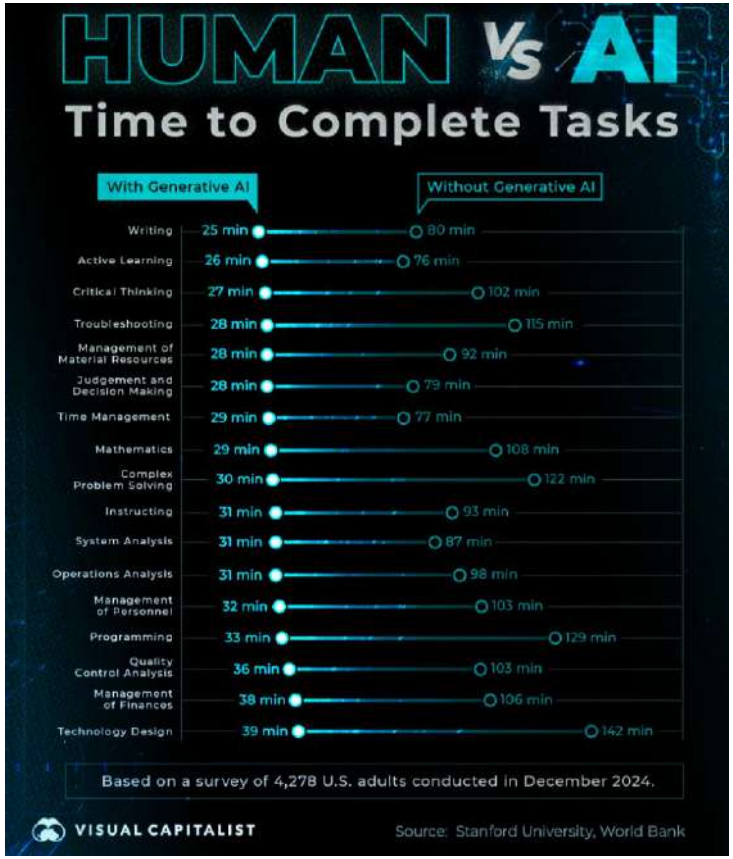
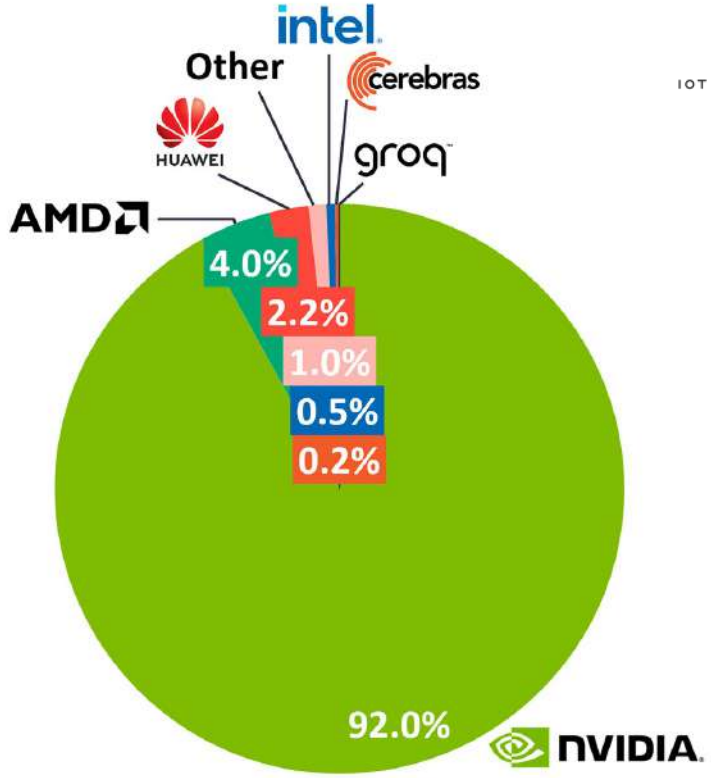
HM Hochschule München University of Applied Sciences

Why do we need open chip design in Europe?

AI: Silicon-Powered Singularity





The Race is not Over, Yet

Perception AI

Generative AI

Agentic AI

Physical AI

Reference from Nvdiai Keynote 2025

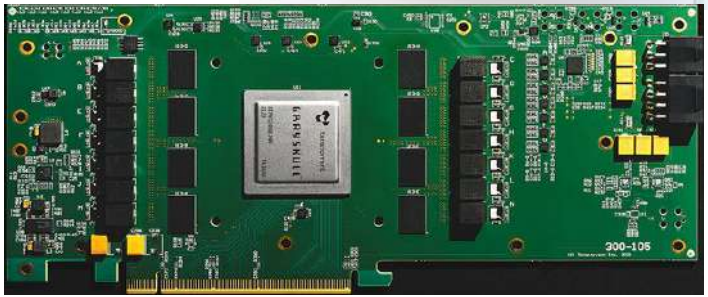
Innovation beyond NVIDIA Gravity

It’s the software. Flexibility key for fast evolution!

Open Standard ISA to counter a monopoly

RISC-V®

RISC-V: The Free and Open RISC Instruction Set Architecture



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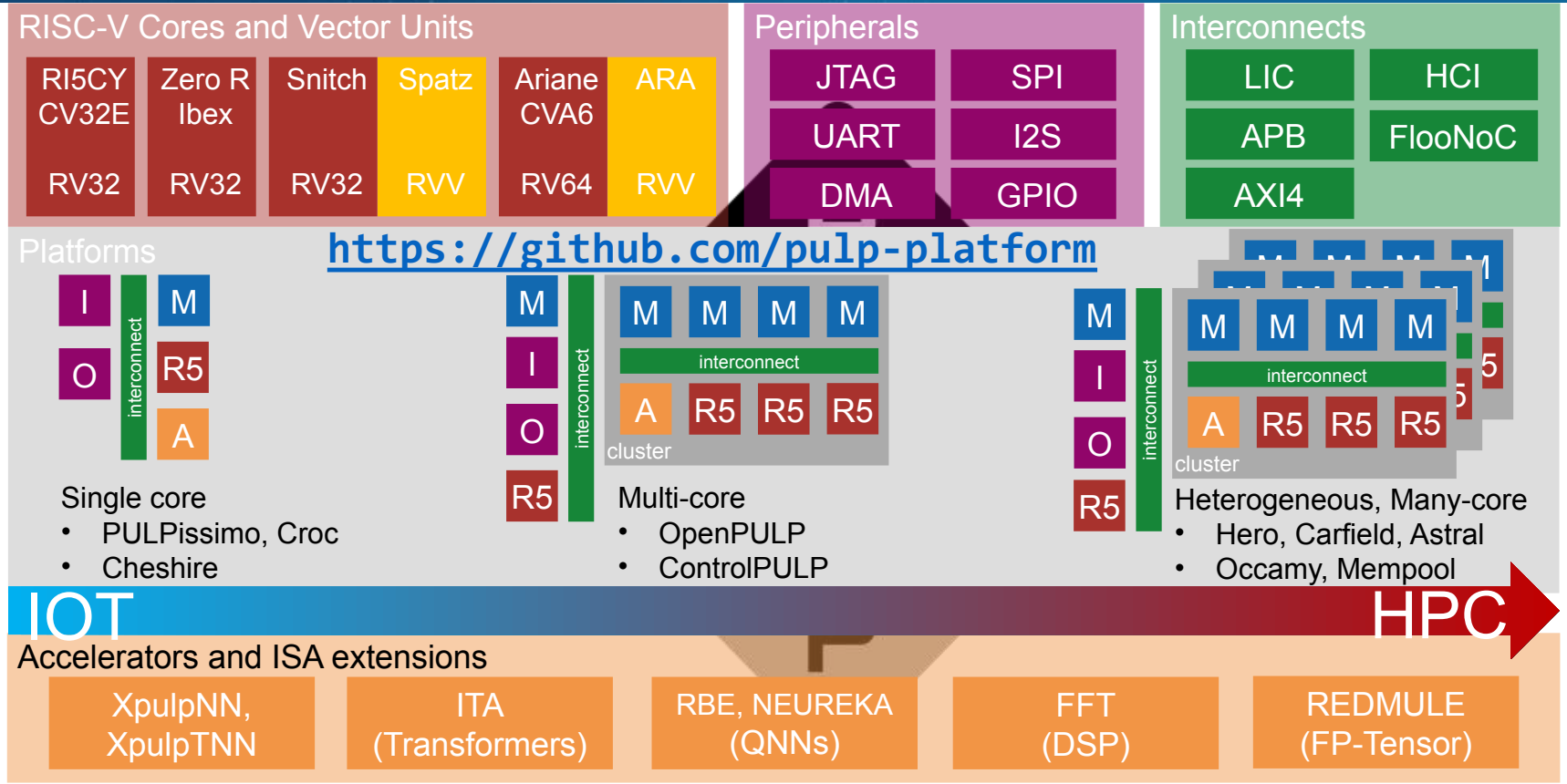
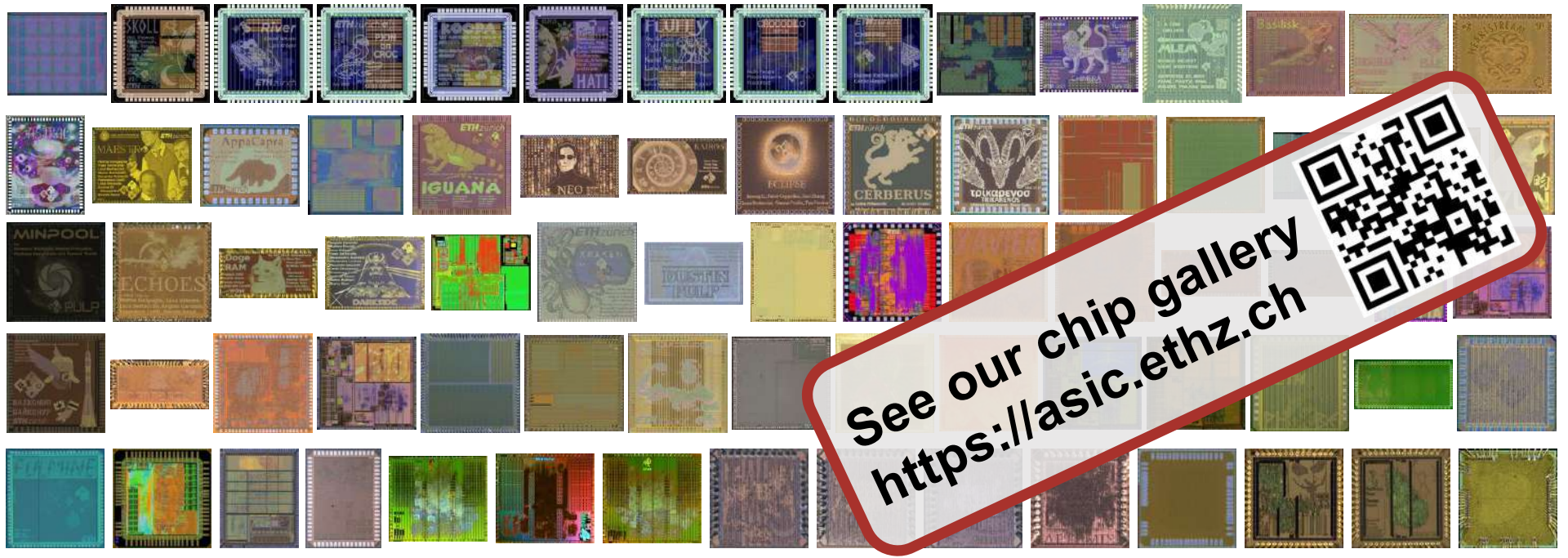
PULP: Open RISC-V Hardware IPs



More than 75 PULP Chips

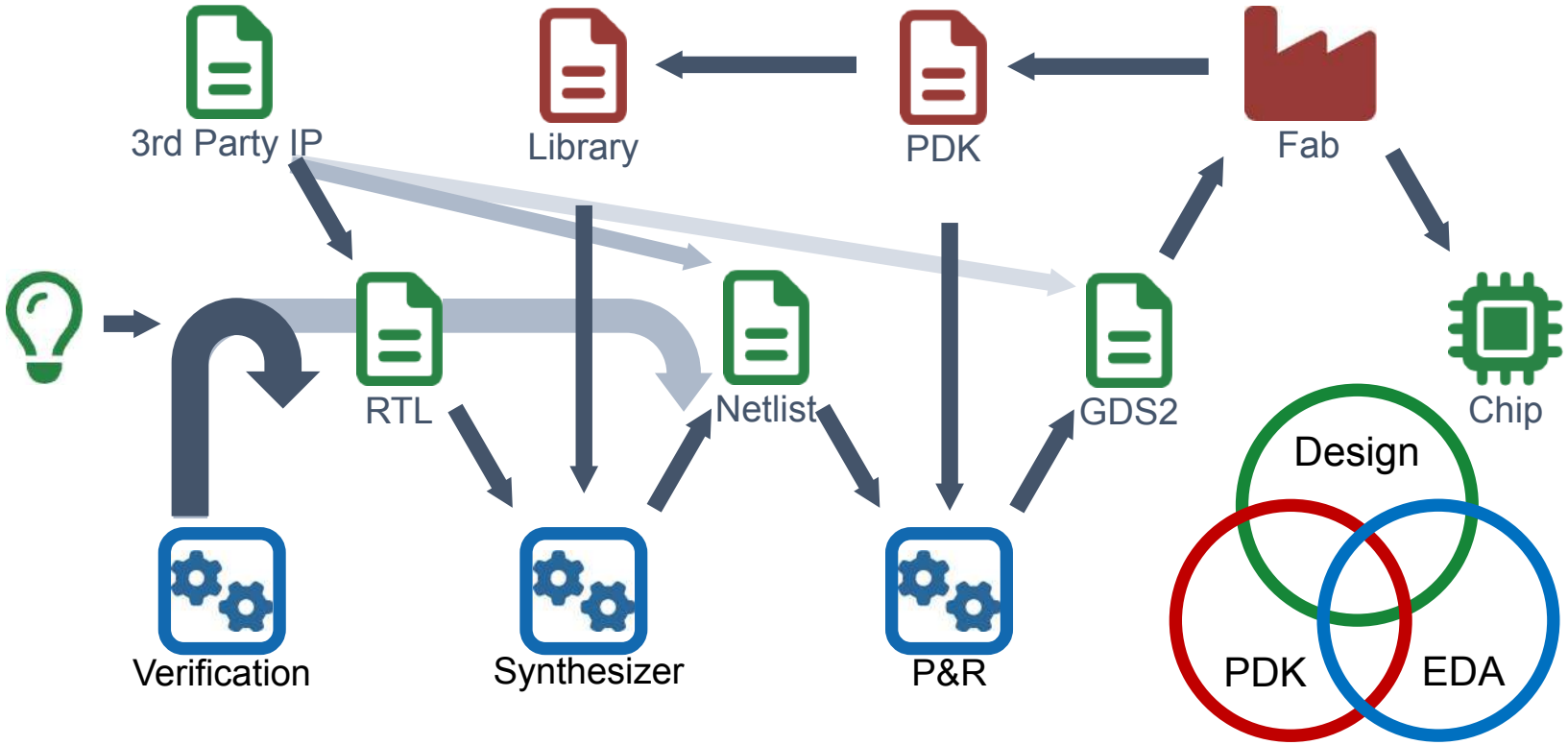


Beyond ISA: Open Chip Design!

- **Boosts research**
  - Open source projects as research infrastructure, build on shared efforts and focus on new ideas
  - More reproductible and more impactful research
- **Democratizes innovation**
  - Lower entry barriers for startups and SMEs
  - Incentivize cross-disciplinary development
- **Contributes to European workforce development**
  - Facilitate upskilling and reskilling
  - Build up expertise and ecosystems of chip designers

But: Building a chip is a complex task with many components and steps

IC design flow



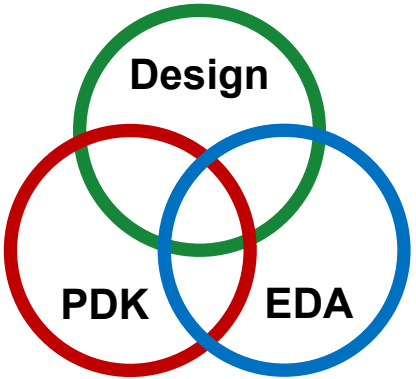
Three Key Parts of the IC flow

Design

- RTL / HDL descriptions (quite common)
- Schematics / Physical Design (may have dependencies to technology information)

Tools (EDA)

- Front-end tools (Design Entry & Synthesis)
- Back-end tools (Placement and Routing)
- Verification tools (Simulation)



Manufacturing (PDK)

- Design rules for manufacturing (separation, minimum width of metals)
- Layer stack information for parasitics (thickness, dielectric constants..)
- Device models (SPICE parameters) for simulation

Open HW IPs are widely available

- (Digital) designs are easily shared in HDL like software over GitHub
- Collaboration models and licensing are established

Big push of RISC-V CPUs

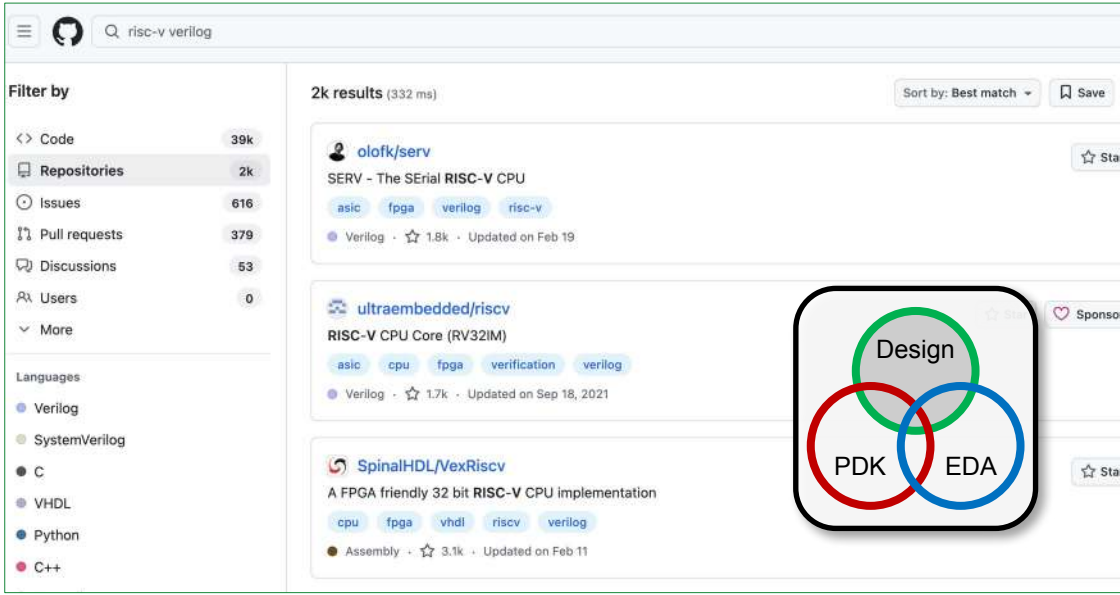
CHIPS ALLIANCE

lowRISC

opentitan

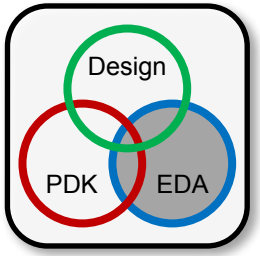
OPENHW GROUP — PROVEN PROCESSOR IP

BOSC



Open Source EDA is Maturing

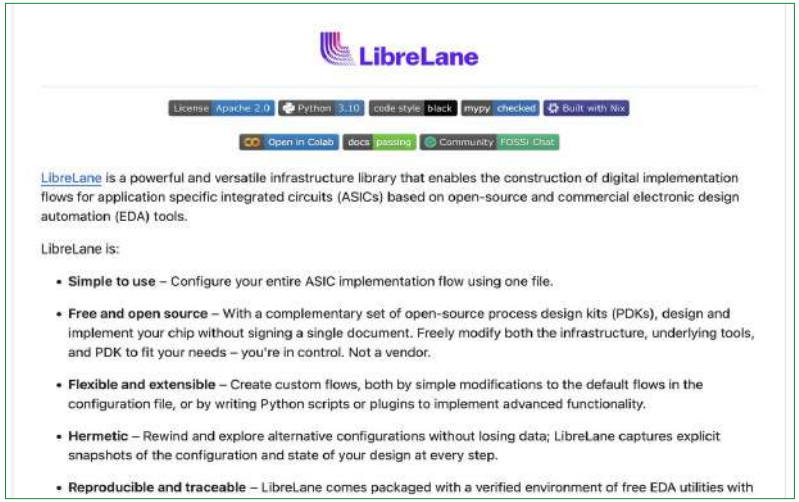
- **Open Source Tools since 1980s (MAGIC)**
- **Large investment by DARPA IDEA: OpenROAD**
  - 24 hour turnaround, fully-integrated digital implementation flow
  - Tools for a complete end-to-end flow
  - Leverage Yosys for synthesis
- **But: EDA is not only synthesis and implementation, also design entry, verification. Popular examples:**
  - Verilator: Widely used RTL simulator
  - Surfer: Novel waveform viewer
- **Leverage open source for:**
  - Increased productivity: Novel approaches, recombine, innovate
  - Integration of custom flows, easy to extend



Reliable Open Source EDA

- **Point tools vs. EDA cockpit**
  - Getting several independent tools to work at the same time is very demanding work
  - Starting fast, without huge setup challenges

Well maintained Docker container



LibreLane

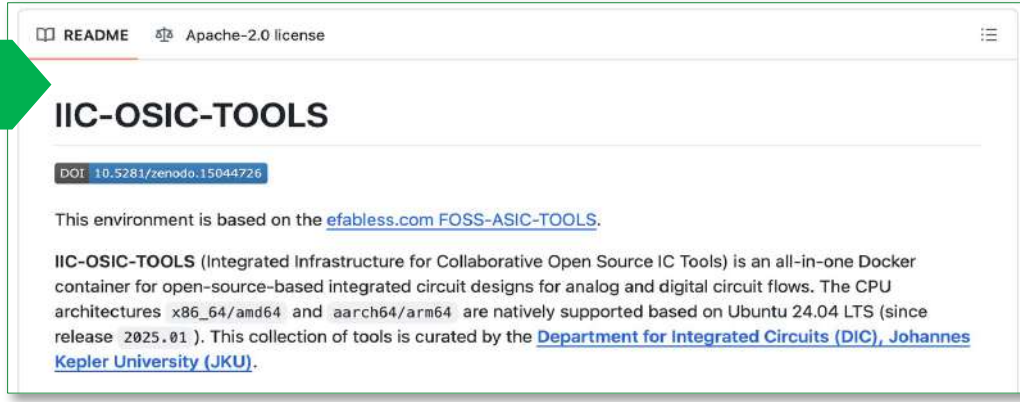
License Apache-2.0 | Python 3.10 | code style black | mypy checked | Built with Nix

Open in Colab | docs passing | Community FOSSi Chat

LibreLane is a powerful and versatile infrastructure library that enables the construction of digital implementation flows for application specific integrated circuits (ASICs) based on open-source and commercial electronic design automation (EDA) tools.

LibreLane is:

- **Simple to use** – Configure your entire ASIC implementation flow using one file.
- **Free and open source** – With a complementary set of open-source process design kits (PDKs), design and implement your chip without signing a single document. Freely modify both the infrastructure, underlying tools, and PDK to fit your needs – you're in control. Not a vendor.
- **Flexible and extensible** – Create custom flows, both by simple modifications to the default flows in the configuration file, or by writing Python scripts or plugins to implement advanced functionality.
- **Hermetic** – Rewind and explore alternative configurations without losing data; LibreLane captures explicit snapshots of the configuration and state of your design at every step.
- **Reproducible and traceable** – LibreLane comes packaged with a verified environment of free EDA utilities with



README | Apache-2.0 license

IIC-OSIC-TOOLS

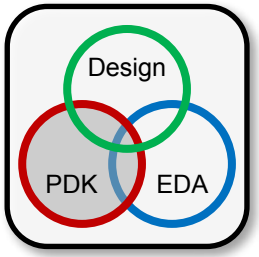
DOI 10.5281/zenodo.15044726

This environment is based on the efabless.com FOSS-ASIC-TOOLS.

IIC-OSIC-TOOLS (Integrated Infrastructure for Collaborative Open Source IC Tools) is an all-in-one Docker container for open-source-based integrated circuit designs for analog and digital circuit flows. The CPU architectures `x86_64/amd64` and `aarch64/arm64` are natively supported based on Ubuntu 24.04 LTS (since release `2025.01`). This collection of tools is curated by the Department for Integrated Circuits (DIC), Johannes Kepler University (JKU).

Easy to use flow, reproducible builds

Open PDKs: Starting



- **Great progress, but choice on mature nodes**
  - Skywater 130nm
  - IHP 130nm
  - Globalfoundries 180MCU
    (a High Voltage technology that uses 500nm transistors)
- **Some are on the way**
  - IC Sprout 55nm (announced, but practical designs still a bit far away)
- **We need more open PDKs to for more relevant designs**
  - Something in the 65nm – 28nm range would be a **game changer**
  - Drafted an open letter to raise awareness with 300+ signatures

https://open-source-chips.eu/

Do we need all Three?

- **Yes, when open sourcing a tech-dependent IP**
  - For 28nm and less clock rates of 500MHz – 2GHz are easily possible
  - An internal clock generator is essential
  - Good luck getting access to a low-cost clocking IP
- **We designed an FLL (Frequency Locked Loop) back in 2016**
  - *D. E. Bellasi and L. Benini, "Smart Energy-Efficient Clock Synthesizer for Duty-Cycled Sensor SoCs in 65 nm/28nm CMOS," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 9, pp. 2322-2333, Sept. 2017, doi: 10.1109/TCSI.2017.2694322.*
  - Ported and taped-out in many technologies: UMC65, TSCM65, GF22, GF12, TSMC7…

People have asked us repeatedly if we could share our FLL

.. and we really want to share our FLL, we know how much it helped

Sharing Technology-Specific IP

- **Assuming you have no objections from your institution to share your IP**

The design requires technology data that is under NDA

- You can not share anything without getting permission from the technology provider
- Usually this requires a multi-party NDA

Design may contain standard cells from a different provider

- You will have to contact the IP provider to ask for permission
- Our FLL for GF22 uses INVECAS standard cell libraries now owned by Synopsys
- In theory you can send a design WITHOUT the cells only references, add the cells locally

You have used EDA tools with academic licenses for your design

- Most academic license agreements would not allow you to transfer the output to others
- You need to contact the EDA vendor and ask for their permission to share

Sharing Technology-Specific IP

- **Assuming you have no objections from your institution to share your IP**

The design

- You can n
- Usually th

Design may c

- You will ha
- Our FLL fo
- In theory y

You have use

- Most acad
- You need t

This is a long and tedious process

On average it takes 6 months

even with great support form everyone involved

Even worse this effort is

needed by the donor every single time

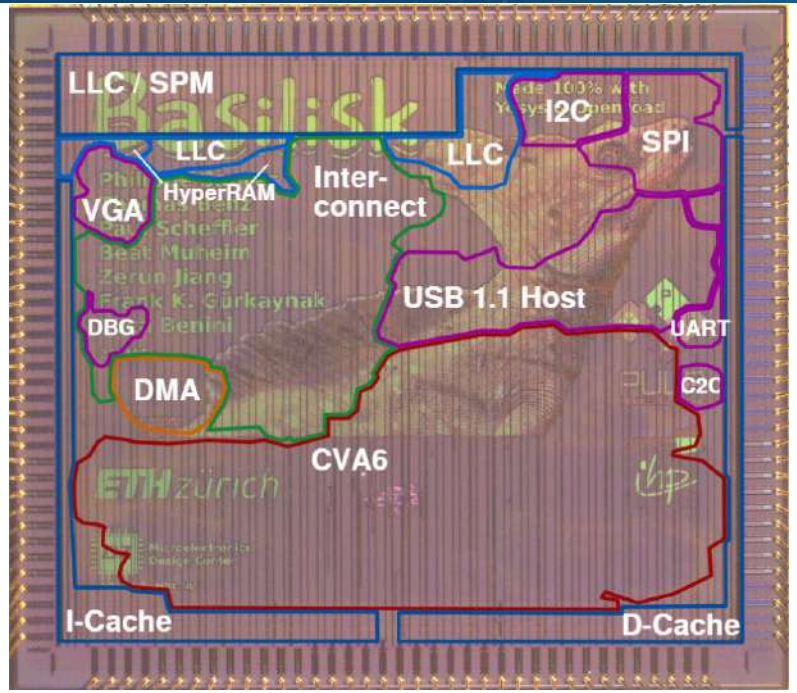
someone wants to use your IP

Open is not the enemy of Closed!

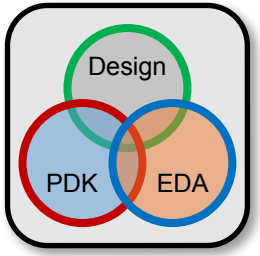
- **OS IP, EDA can coexist with closed IP, EDA → mixing is possible/desirable**
- **OS Lower entry barriers → more SME customers for Closed**
- **OS EDA, IP facilitate research and skill development → eases shortages**

Reality Check 1:
Can we design a Competitive MGate SoC End-to-End Open Source?

Basilisk: Open RTL + EDA + PDK

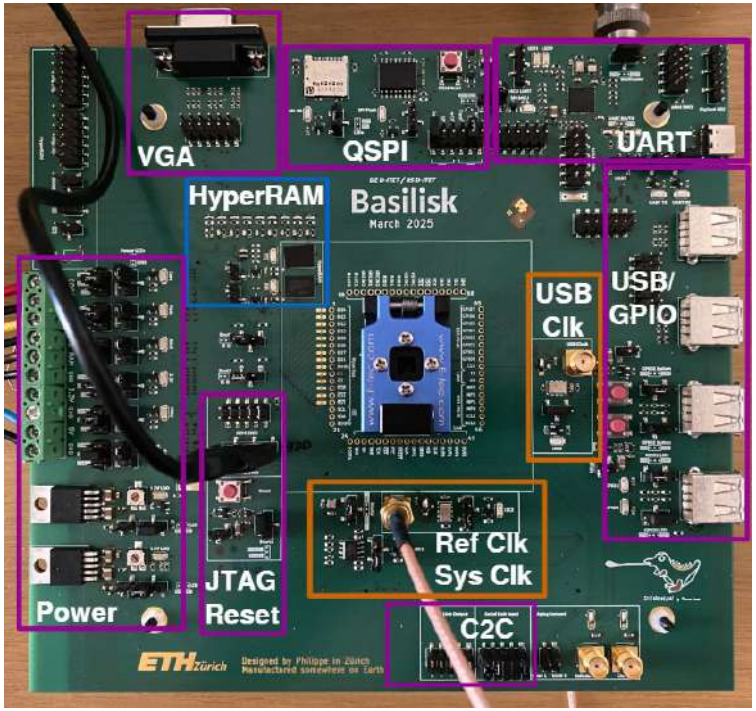


- **Designed in IHP 130nm OpenPDK**
  - **34mm² (6.25mm x 5.50mm)**
  - **~5× larger than previous end-to-end OS designs**
    - **2.7 MGE total, 1.14MGE logic**
    - **24 SRAM macros (114 KiB)**
  - **62MHz at nominal voltage (1.2V)**
- **RV64GC design runs Linux**
- **Active collaboration with**



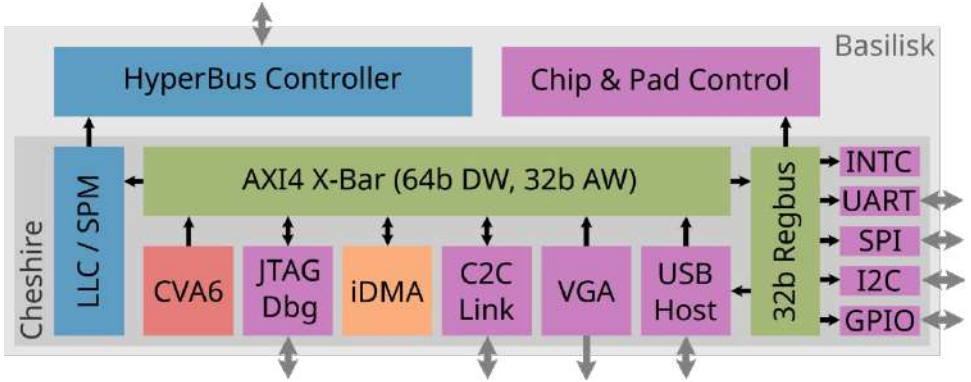
github.com/pulp-platform/cheshire-ihp130-o

Basilisk: Open RTL + EDA + PDK



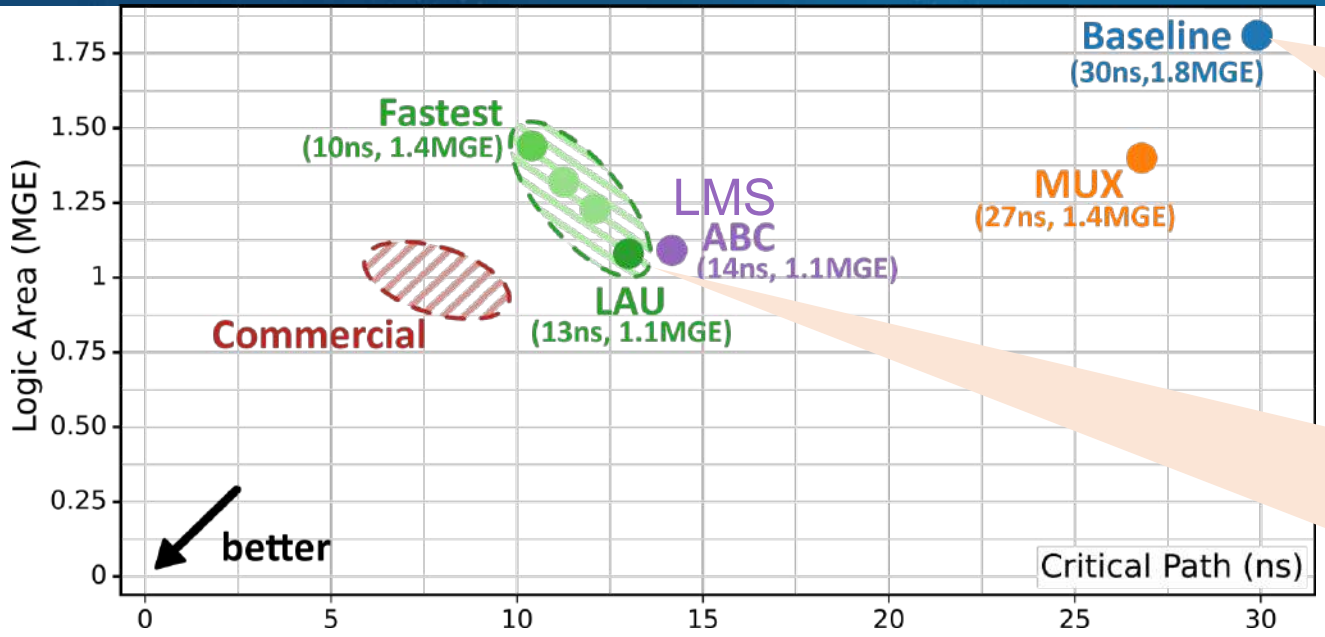
- 64-bit RISC-V core
- Rich peripherals:
  - HyperRAM controller @154MB/s
  - C2C AXI-Link @77MB/s
- Automatic boot via scratchpad

Watch the video



arxiv.org/pdf/2505.10060

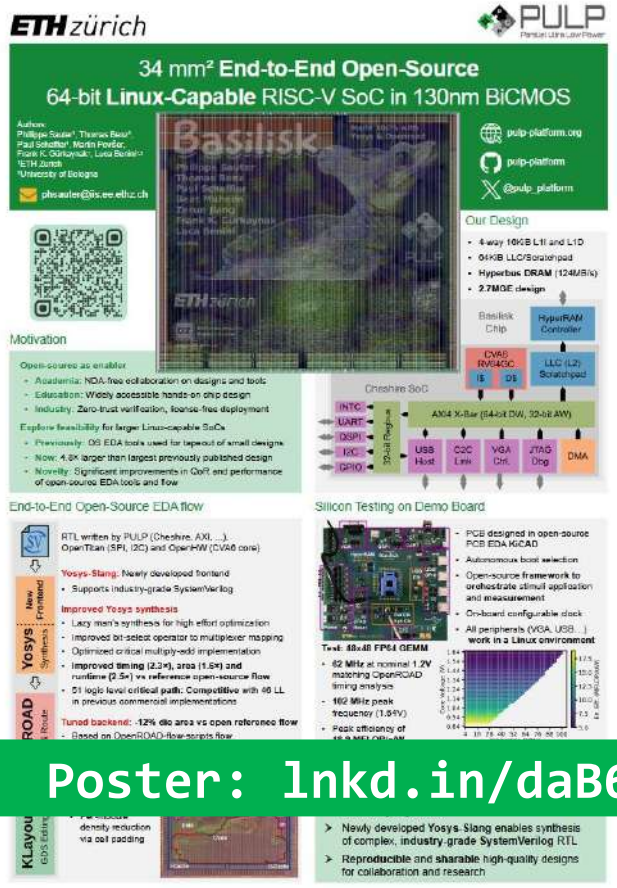
Is Basilisk Competitive?

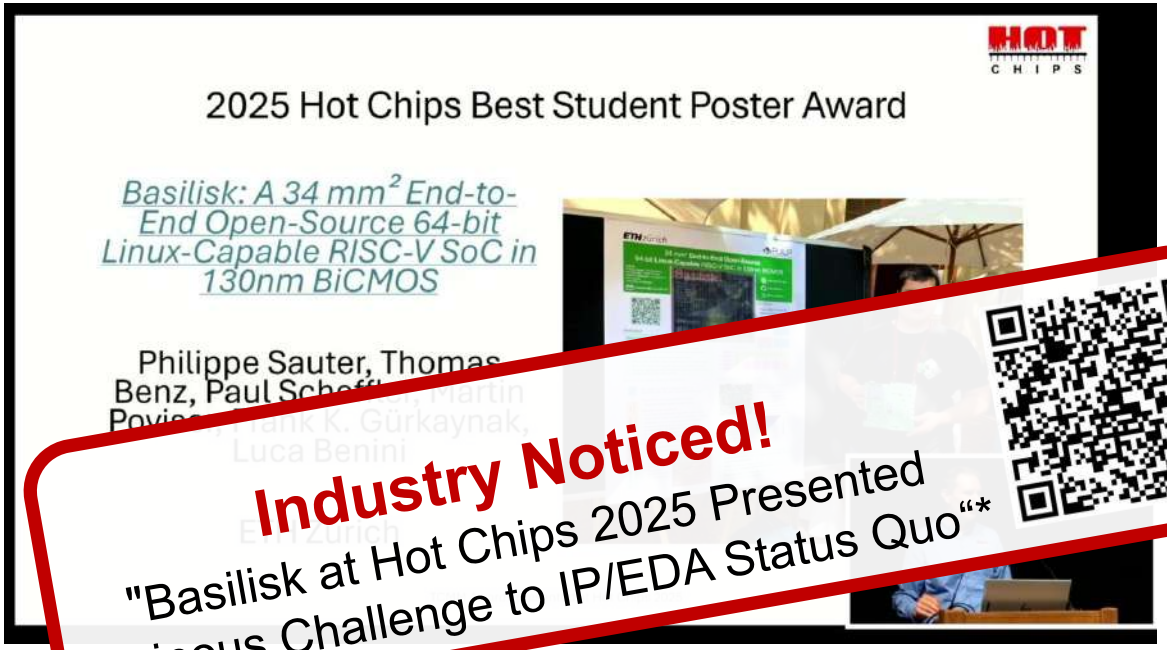


Yosys-slang full Sysverilog Frontend: @ <6sec runtime (from minutes)
Yosys synthesis: 1.1 MGE (1.6×) @ 77 MHz (2.3×), 2.5× less runtime, 2.9× less RAM
OpenROAD P&R: tuning -12% die area, +10% core utilization

Commercial EDA leads, but OS-EDA IS usable, now!

Basilisk at





Industry Noticed!

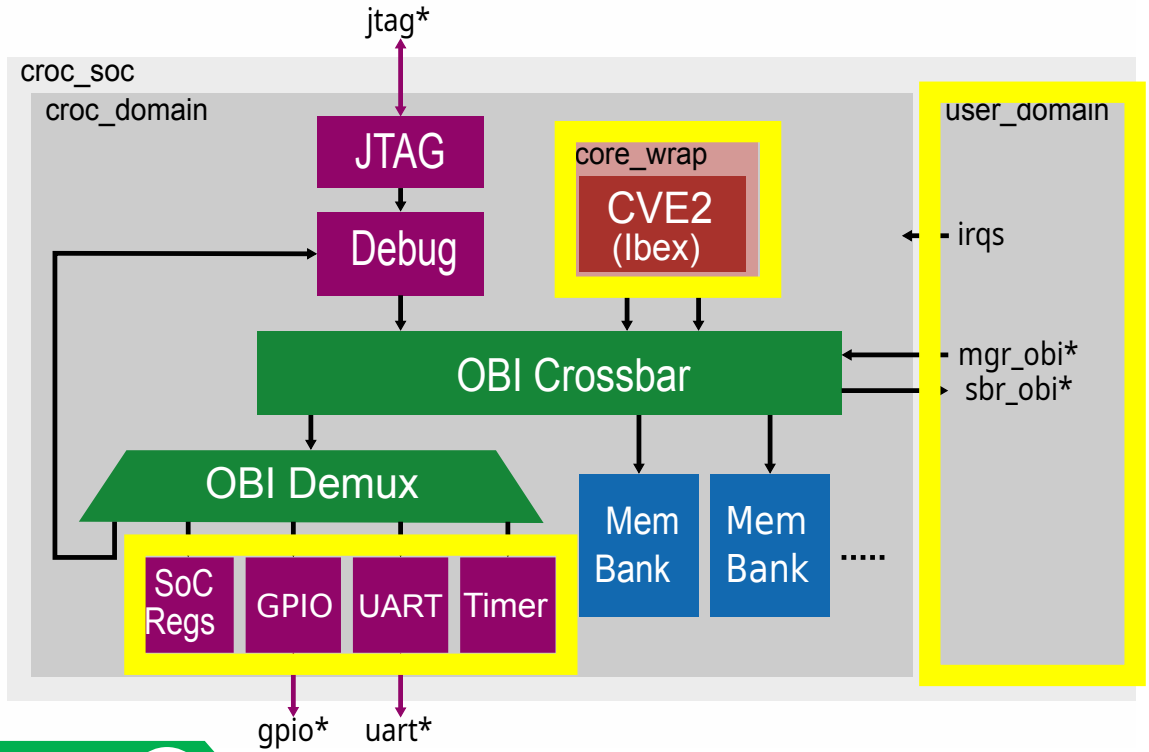
"Basilisk at Hot Chips 2025 Presented Ominous Challenge to IP/EDA Status Quo"*

*semiwiki.com/ip/risc-v/361204-basilisk-at-hot-chips-2025-presented-ominous-challenge-to-ip-eda-status-quo/

Reality Check 2: Can we Build a Higher Education Path on End-to-End Open Source?

Croc: A SoC for education

- 32-bit RISC-V core (CVE2)
- Options to improve
  - User domain
  - Adding peripherals
  - Extensions to the core
- Reference design for VLSI2 lecture and exercises
- Pipe-cleaning with two Croc-based tapeouts
  - Mlem, Koopa (next slide)



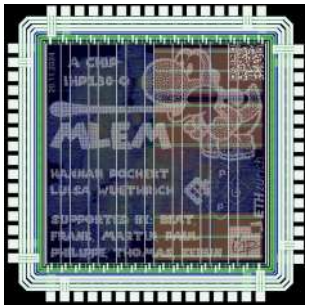
github.com/pulp-platform/croc

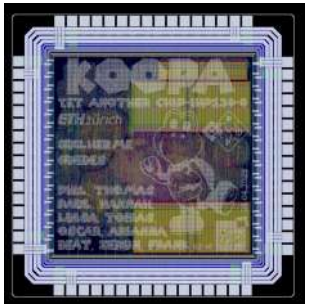
Teach IC Design using OS HW

- **Since 2015 our VLSI courses are using open flows**
  - **IHP130, Yosys, Open Road**
    - some parts still using commercial EDA will be gradually replaced
- **All teaching material online**

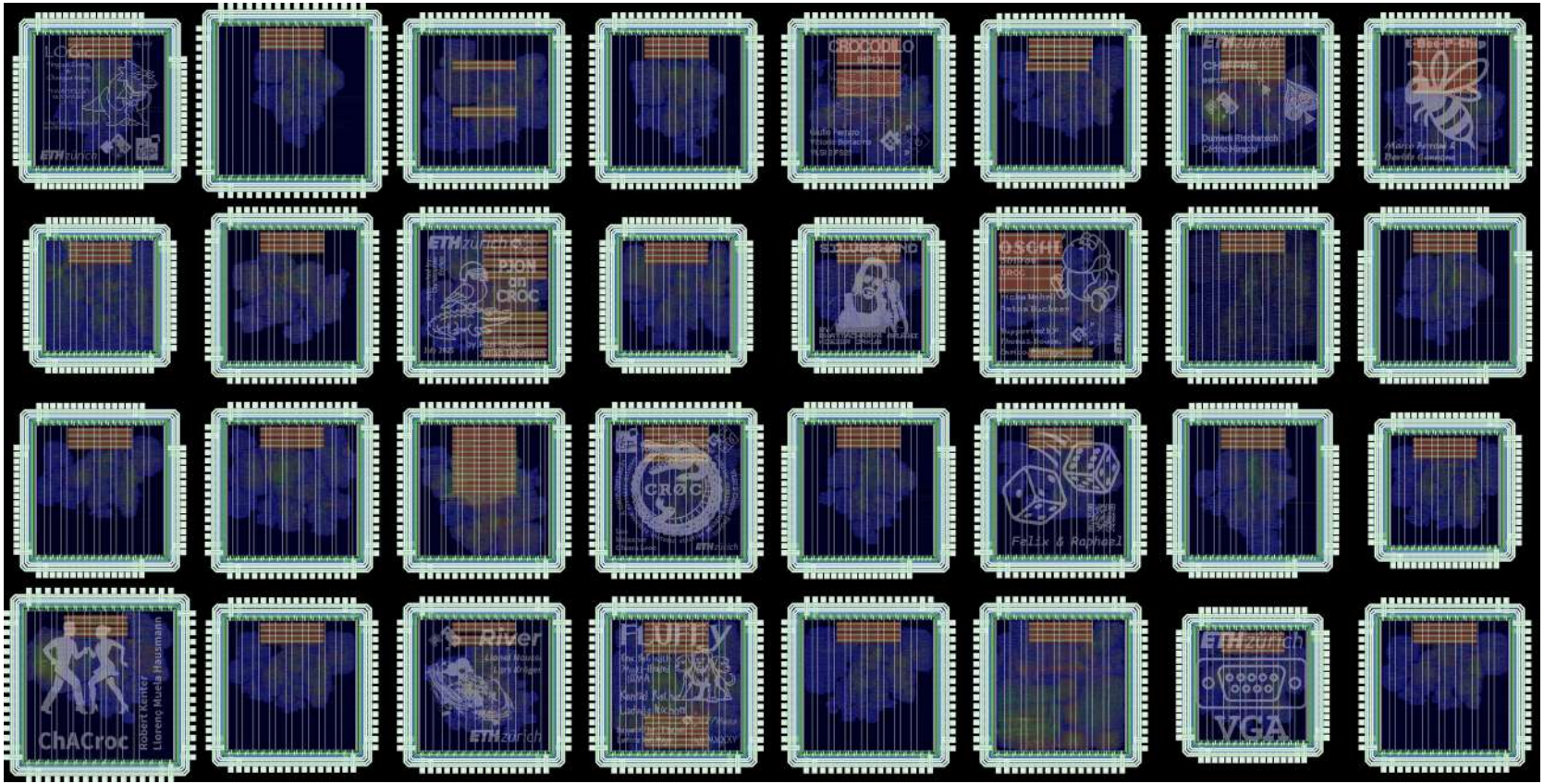
`https://vlsi.ethz.ch`

- **Project based grading**
  - Students work in groups of 2
  - Enhance CroC SoC
  - Best designs are taped-out
- **Already in its second year**





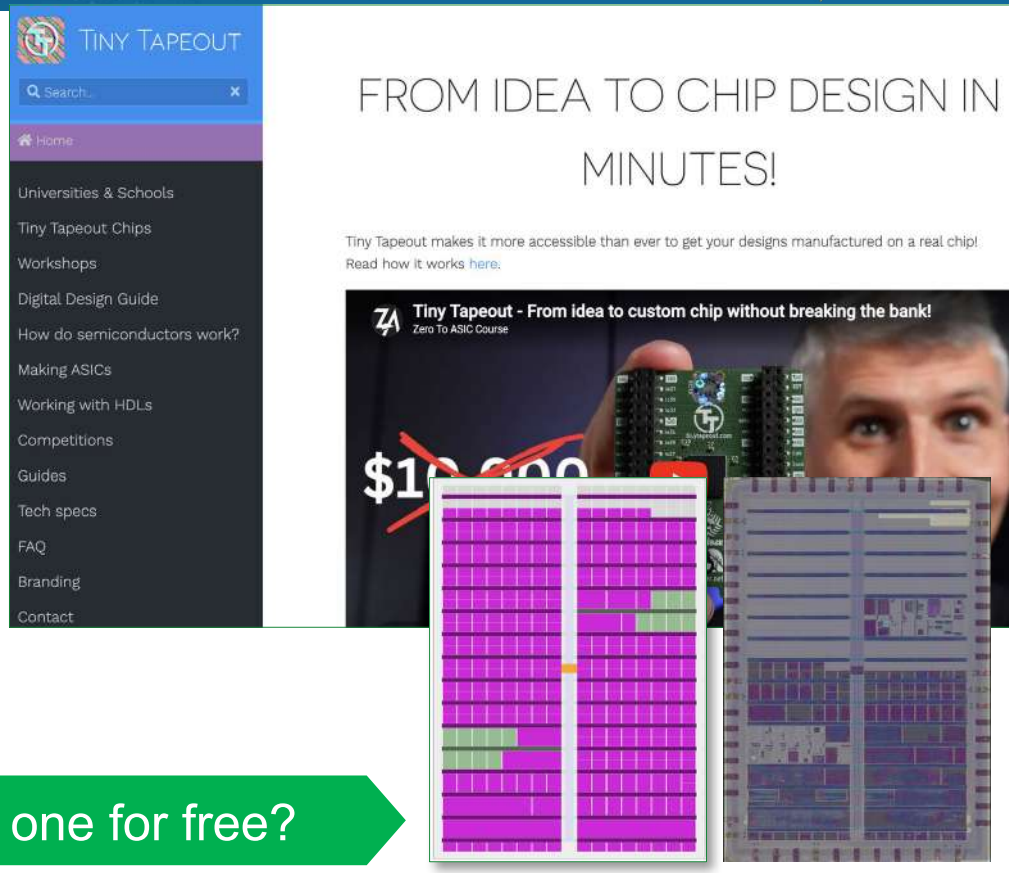
…And the students delivered!



Reality Check 3:
Is Open Source Helping Silicon Democratization?

Tiny Tapeout

- **Idea: Split MPW area into tiny tiles**
  - Multiplexer harness
  - Shared design with selection logic
  - Analog designs and pins supported
- **PCBs available with chip**
- **You get ALL open designs on chip**
  - Not only your design
- **Starting at**
  - **185 €** individuals
  - **385 €** academic/industry



Shouldn't every student in Europe get one for free?

Open IC Design is already working

Competitive & reproducible

- Performance claims can be verified
- Non-trivial designs are possible
- Generate example datasets that can be used for training

Easier collaboration / sharing

- Stand on the shoulder of giants
- Share common parts that all need
- Concentrate work where it matters

Reduce entry barriers for all

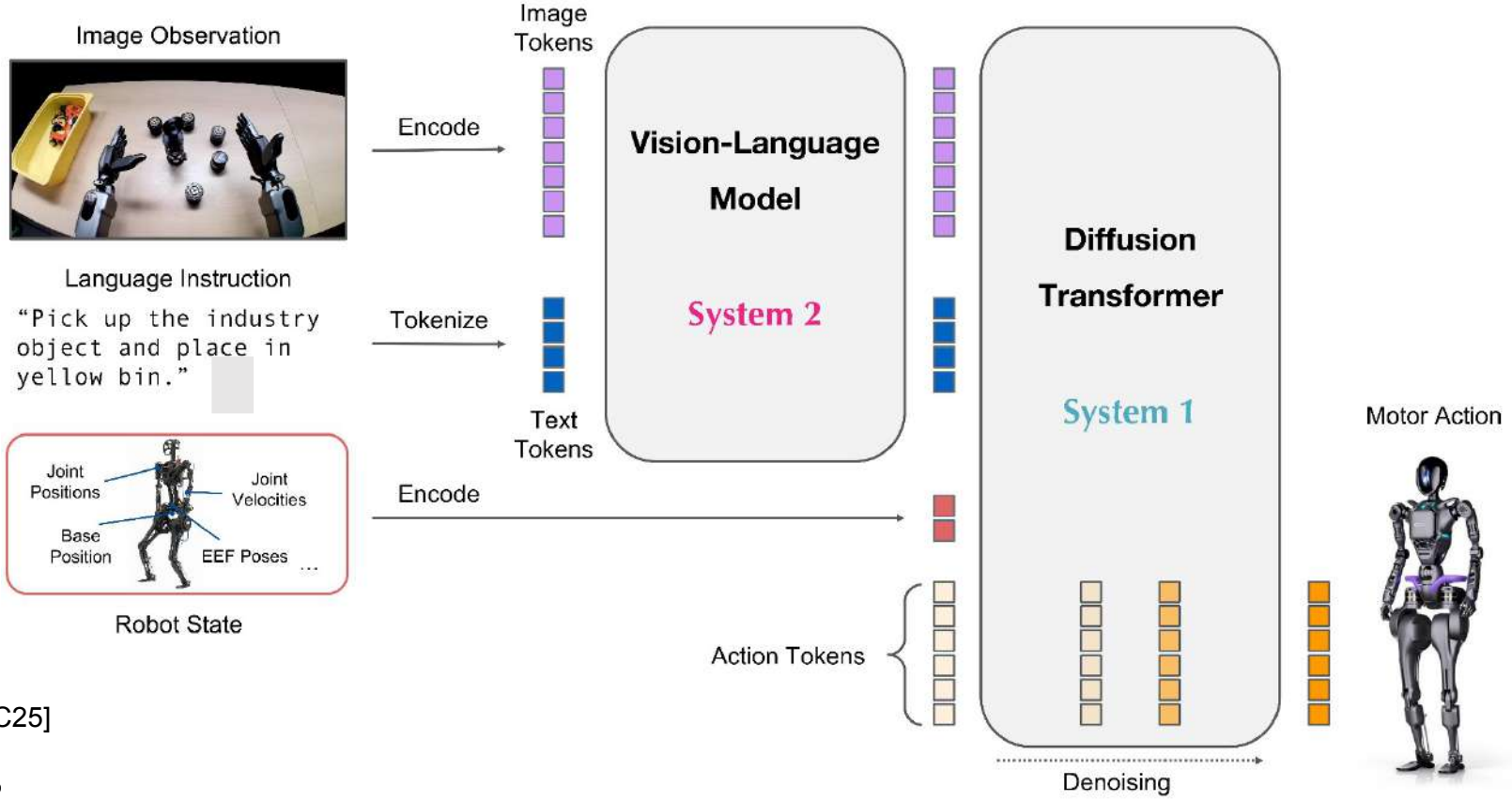
- Get started with IC Design easily
- No agreements needed to get started
- Can then decide to stay open or not

Accessible teaching for all

- Share courses, designs, examples
- Create tutorials, knowledge bases
- Training for industry

Reality Check 4:
Can Open Source Hardware help in the Physical AI Race?

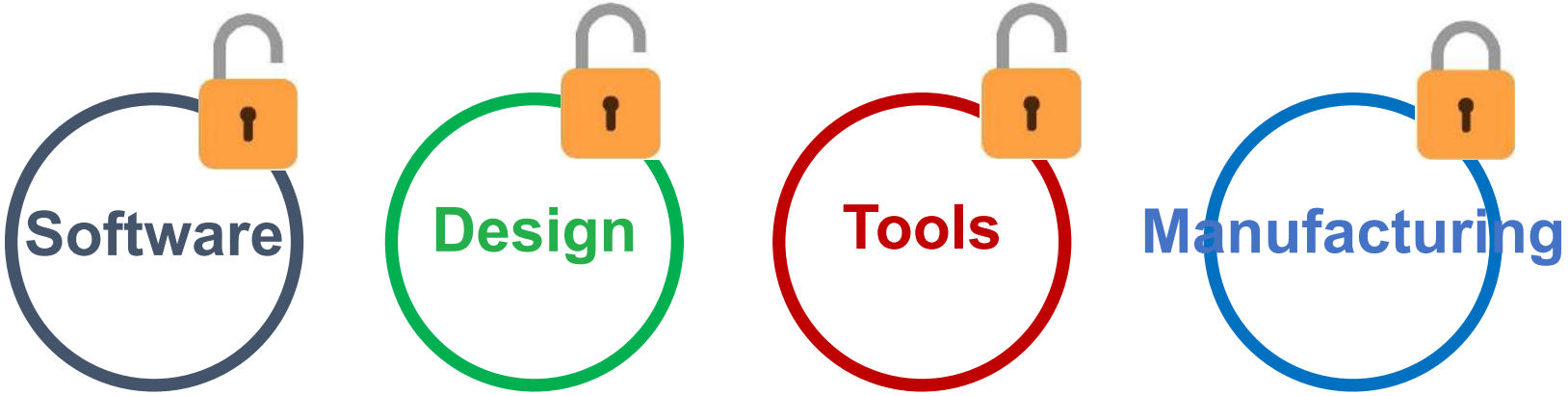
Physical AI ☾ Scale & Efficiency



[GTC25]

Open EDA: Chips in Advanced CMOS?

Extreme Performance + Energy Efficiency is required!

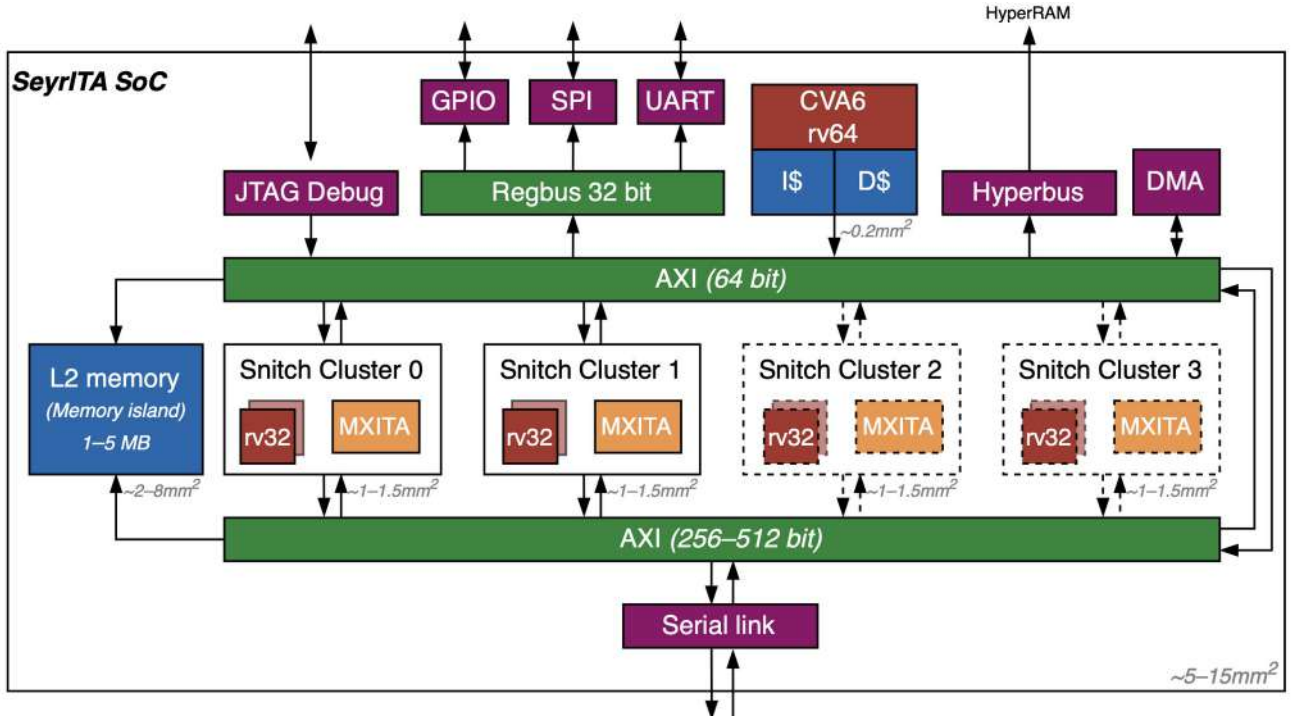


HW-SW Co-Design

HW-SW & Tools Co-Optimization

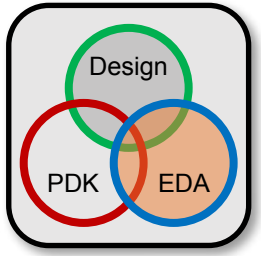
Get the best from advanced nodes!

SeyrITA: open Physical AI SoC



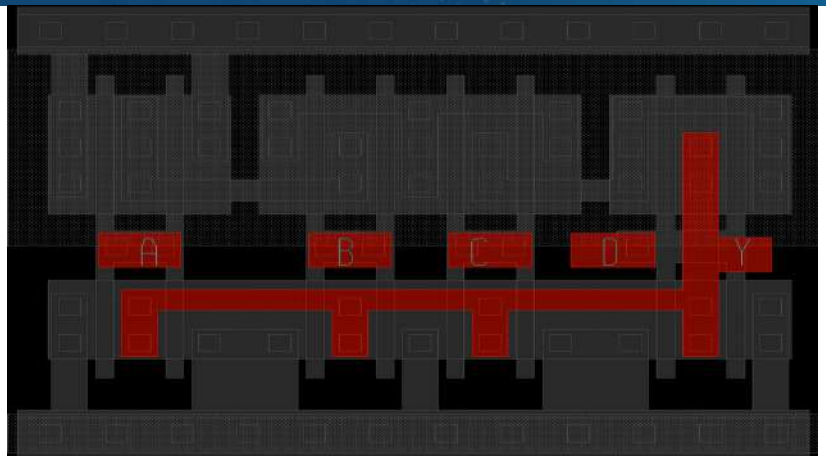
GlobalFoundries™

- **Challenging work**
  - Large design, modern technology
  - Encounter problems daily
  - We try to solve them one problem at a time
  - Confident we will get it done

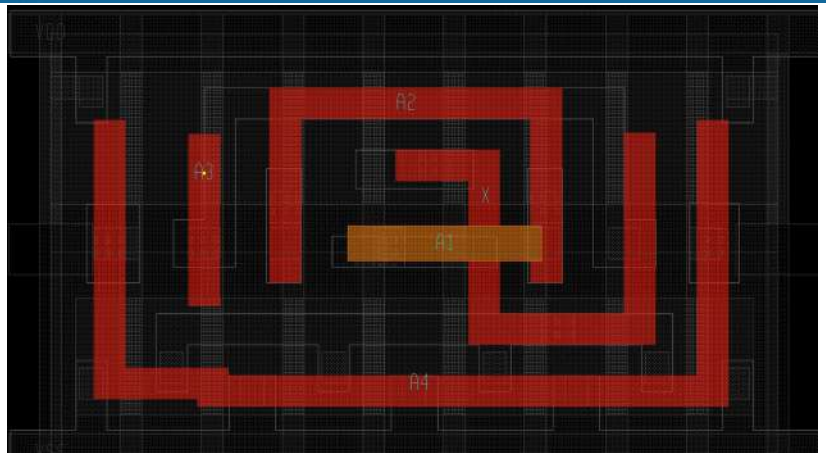


https://github.com/pulp-platform/ita

Old vs Modern Nodes: Standard Cells



IHP130 NOR4 Cell 5.76µm x 4.22µm



GF22 NOR4 Cell YYµm x ZZµm

IHP 130 cells

- Larger with lower density
- Simple pin shapes

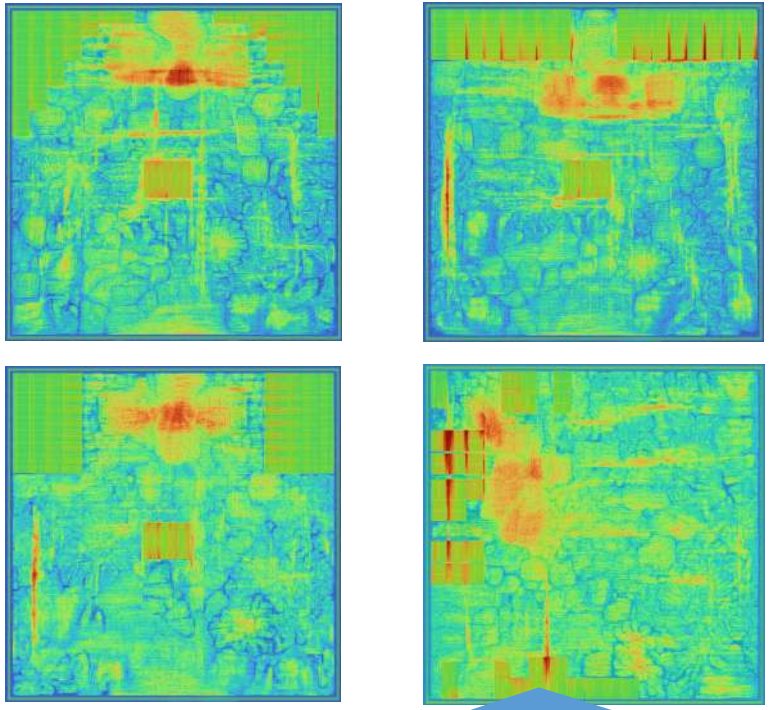
GF22 FDX cells

- Smaller and denser
- Irregular pin shapes

Much more complex Synthesis and P&R tooling!

Working on SeyrITA Tapeout

- First large 22nm tapeout with open-source tools
- Improve tools and close the performance gap
- Identify and implement missing features along the way
- Active Collaboration with

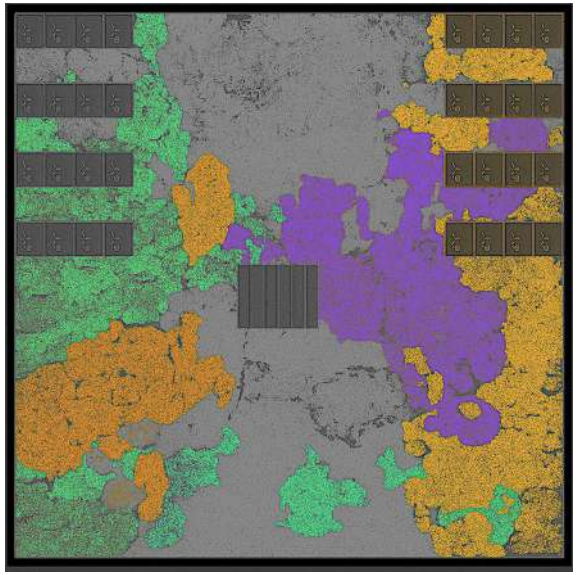


Cluster floorplan exploration

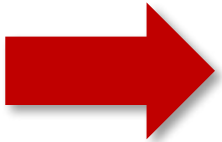
Significant Improvements in QoR

- Tool fixes and improvements & **aggressive hyperparameter tuning**
- All leading to **56% higher frequency** and **42% area reduction!**

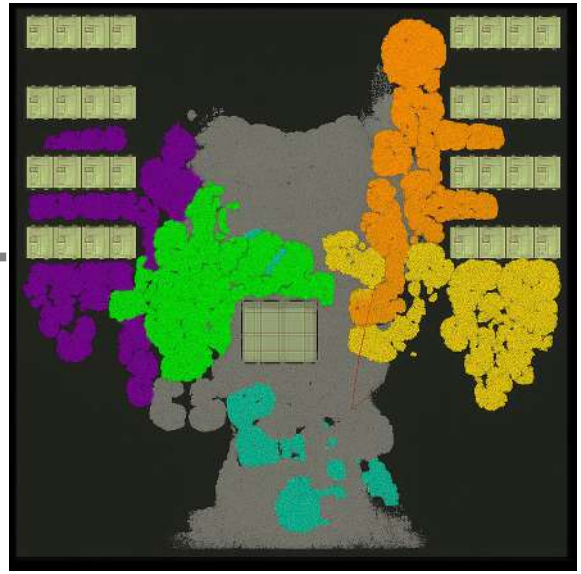
Baseline



231 MHz
7.7 MGE



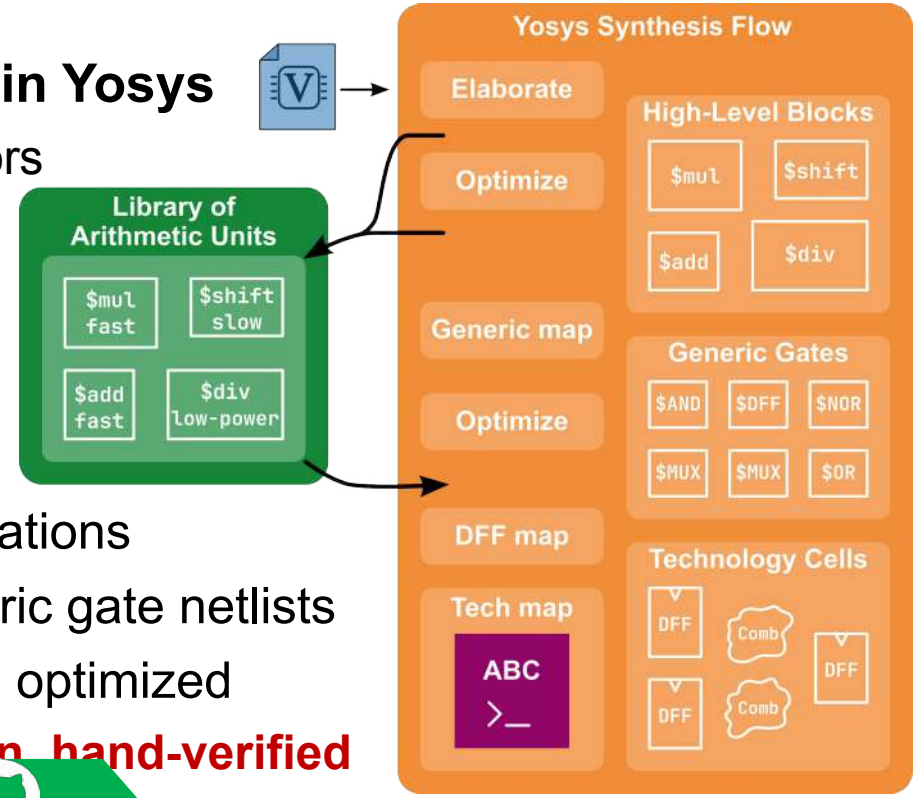
Optimized



360 MHz
4.5 MGE

Library of Arithmetic Unit (LAU)

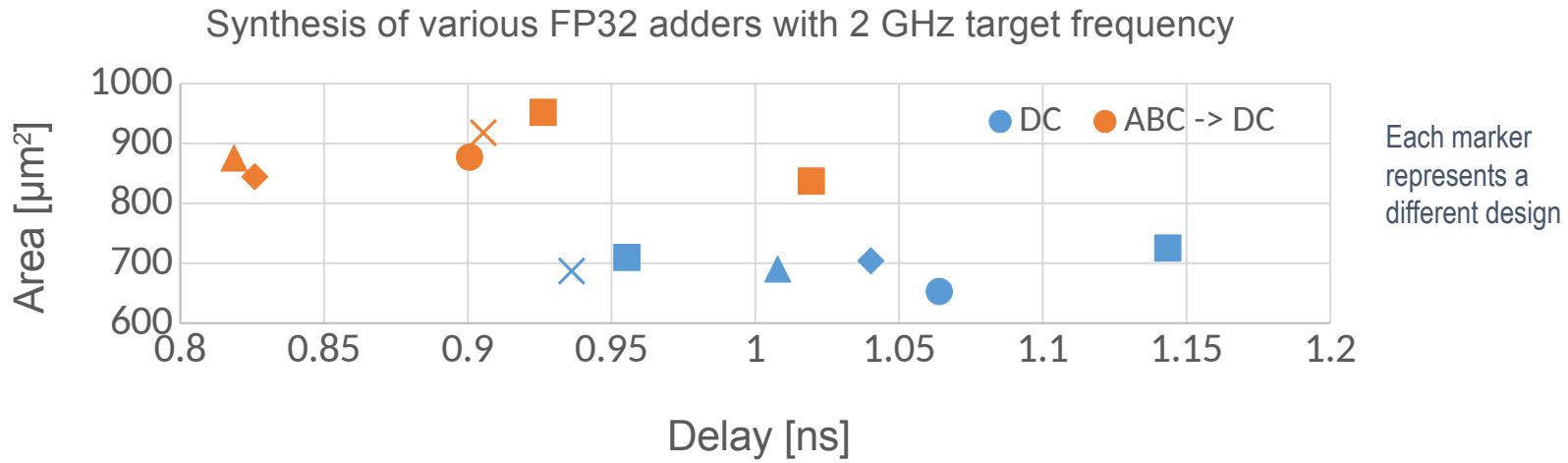
- **Block replacement is implemented in Yosys**
  - Detect and replace arithmetic operators
  - Currently: manual selection
  - **Next: algorithmic, AI based!**
- **No open-source library**
  - **We built rich optimized library**
    - A wide range of arithmetic operations
    - 3 performance variants of generic gate netlists
    - Thoroughly QoR evaluated and optimized
  - **SV port from VHDL; LLM translation, hand-verified**



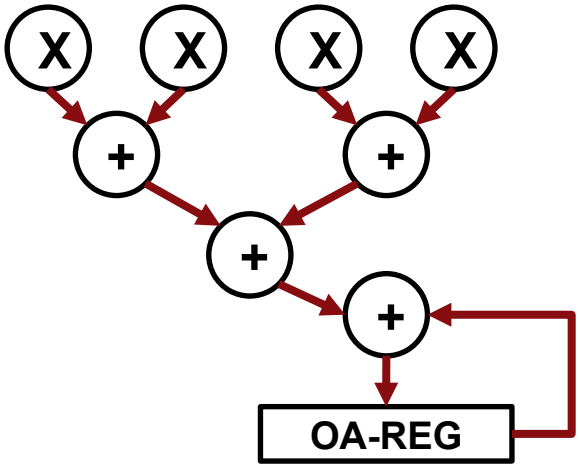
github.com/pulp-platform/elau

There is still room for improvement

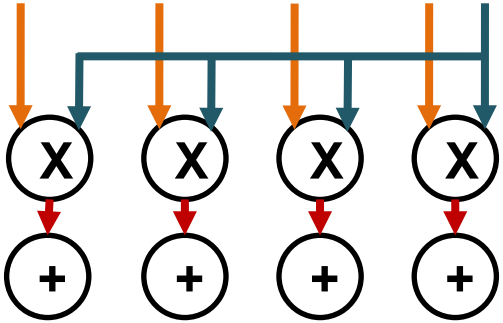
- **Explored various FP32 adders:**
  - Applied ABC logic optimizations before Synopsys Design Compiler synthesis, leading to higher frequency Pareto points for several designs.



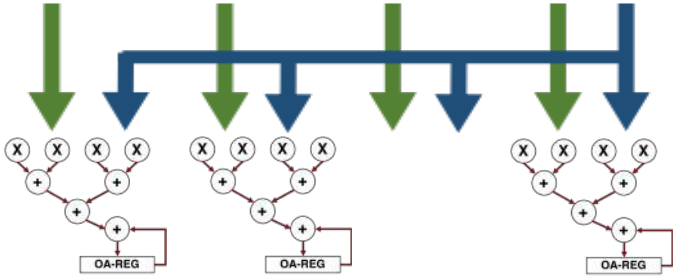
Specialization + EDA multiplicative effect



Inner Product



Outer Product



Mixed

Precision tuning – OP/Mem tuning - deep arithmetic optimization – operand network tuning...

Co-Specialize SW, HW, EDA & Technology is the frontier

This is why we need more open source chips in Europe

Get to More OS Chips in Europe

- **Various advocacy activities**
  - **Open Letters to support and guide policy makers**
  - **Roadmap on open source EDA, led to call**

Importance of Open-Source EDA Tools for Academia

Open Letter on European Strategic and Funding Directions

To Whom It May Concern

March 8, 2024

The recent semiconductor shortage and shifts in global political relations have changed the European roadmap on semiconductors and chip design significantly. A mix of incentives for new fabrication facilities for advanced technologies and the ambitious goals to (re)-build leading-edge chip design capabilities in Europe are key cornerstones of the European Chips Act. Under this impulse, various funding actions have been successfully launched, for instance in the area of the creation of IP based on the RISC-V instruction set.

Universities have to be an integral part of Europe's ambitions and are heavily involved in research activities on various levels. This is crucial for two reasons: First, they are incubators of innovative ideas. Second, and equally important, they are of key importance to educating future generations of chip designers and related jobs. The high demand for an increased workforce can only be satisfied with tight coordination and the best support of universities. In these efforts, we believe that open source is a key success factor. The availability of open-source RISC-V IPs developed in

Recommendations and Roadmap for Open-Source EDA in Europe

Version: November 19, 2024 - Public Release

Open Design Environment for European Chips

- **ODE4EC initiative supports a healthy open source ecosystem**
- **HORIZON-JU-CHIPS-2025-IA-EDA-two-stage proposal**
  - 20MEUR funding from EU, total project 50MEUR
  - Organized in three sub projects: Digital, Analog, Productivity
  - Currently in Grant Preparation Phase.
  - Start in May/June 2026, more details to follow
- **Large consortia**
  - 24 partners (DIG), 27 partners (AMS), 24 partners (PIV)
  - From 14 Countries
    (AT, DK, FI, FR, DE, GR, HU, IT, LT, PT, SI, ES, SE, SE, CH, UK)
  - Includes broad participation from most open source contributors **in EU**

ODE 4 EC

ODE 4 EC | ODE 4 EC | ODE 4 EC

DIG AMS PIV

https://ode4ec.eu

Great opportunity to make a difference!

Five lessons from our experience

- **Open source is needed to share designs and ideas efficiently**
  - And we can not build everything ourselves, modern SoCs are way to complex
- **Sharing beyond RTL level requires both open EDA, and open PDKs**
  - There are several roadblocks that prevent sharing in IC Design
  - These can only be addressed once there are PDKs that allow sharing
- **End-to-end open-source flows can already deliver complex working chips**
  - There is a gap to commercial EDA, but it is less than what people think
- **End-to-end open-source flows are great for training and teaching**
  - Being able to share all aspects of the flow allows us to make materials available to everyone
- **There are many interesting opportunities for open EDA**
  - There is more to do than just replicate what proprietary EDA has been doing
  - Opportunities for disruptive developments that will push performance beyond current levels

Save the Date

DATE 26

Leading open source silicon conference

- **ORConf 2026**
  - **September 11 to 13**
  - **Ghent, Belgium**
- **Meet the community**
- **Learn about ODE4EC**
  - Project meeting (in preparation)
  - Following ORConf
- **Free to attend**

"Summer in Ghent" by VisitGent CC BY-NC 2.0

Thank You

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Not the enemy of proprietary EDA

- **Open-source EDA allows developing skills needed for EDA companies**
- **Allows EDA companies to concentrate efforts on differentiating features**
  - i.e. no need to develop waveform viewers
- **Lowering barriers: OS EDA allows you to experiment before investing**
  - Experimenting IC Design: identify the gaps, judge the benefits
  - The more SMEs that venture into IC design the more EDA licenses will eventually be sold.
- **Limit no longer license costs but available CPUs**
  - Makes public (or cross partner) CI flows much easier
  - Many iterations (with small variations): extreme design space exploration
  - Early evaluations of technical choices do not require signoff accuracy