Towards Reliable Systems: A Scalable Approach to AXI4 Transaction Monitoring

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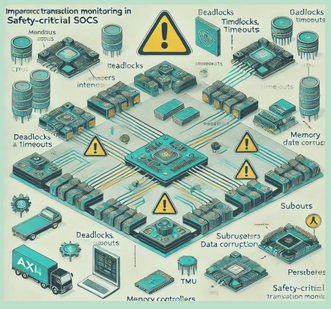
1 Motivation

- **Reliability in safety-critical SoCs**
  - **Robust transaction monitoring** prevents **protocol violations** and **timeouts**, ensuring system integrity
- **AXI4's complexity**
  - **Multiple transaction IDs and multiple outstanding transactions** boost performance but risk **deadlocks, data corruption, and protocol mismatches**
- **Limitations of existing approaches**
  - **Imprecise tracking, timeout-focused,** offer **limited error analysis**, leading to **inadequate fault coverage** and **inefficient fault recovery**

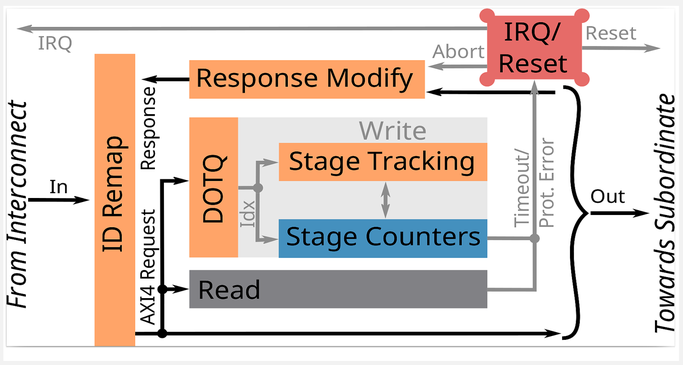


➢ The **Transaction Monitoring Unit (*TMU*)** is a **scalable AXI4 monitoring IP** that enables **real-time failure detection** and **accelerates fault recovery**, offering **configurable trade-offs** between **area efficiency** and **monitoring granularity**

2 TMU Architecture

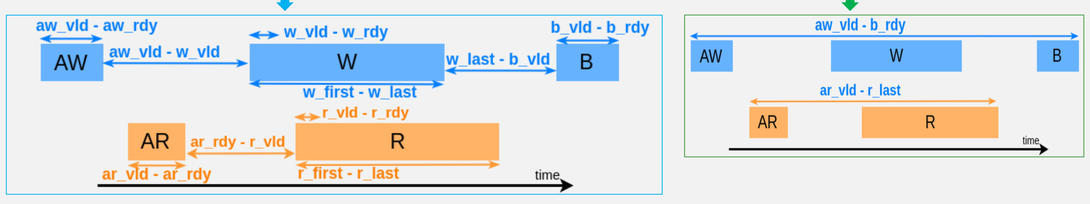
Architecture Components

- **ID Remapper** optimizes ID utilization
- **Write and Read Guards,** each with**:**
  - **DOTQ** manages multiple outstanding transactions
  - **Stage Tracking** monitors transaction progress and validates protocol rules
  - **Stage Counters** measures latency and detects timeouts (configurable prescaler)
- **Response modifier** adjusts and overwrites responses before sending them back to the manager.



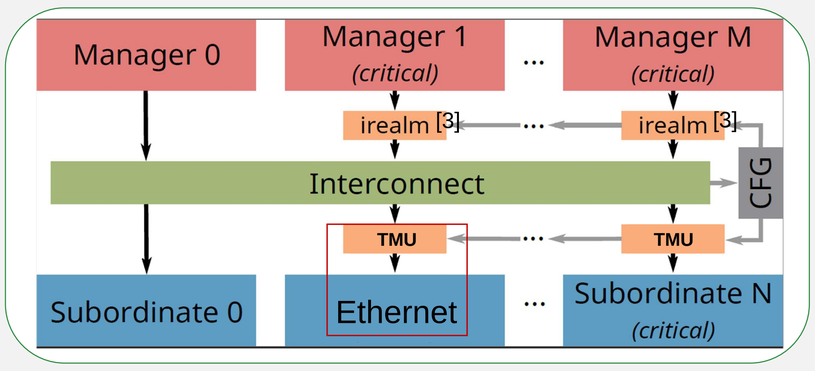
Two variants

Full-Counter (FC)	Tiny-Counter (TC)
Fine-grained tracking across stages within transactions	single counter per transaction
Early fault detection and precise latency analysis	Minimal area overhead

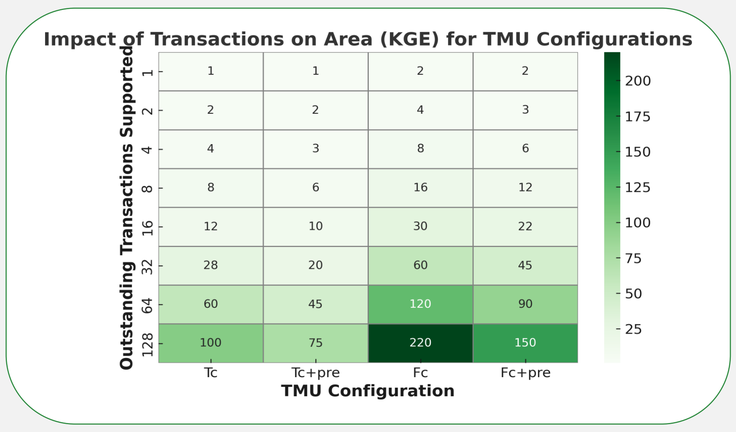


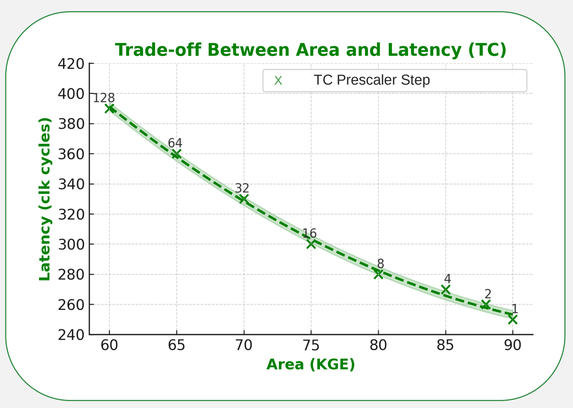
3 Full-Stack Evaluation

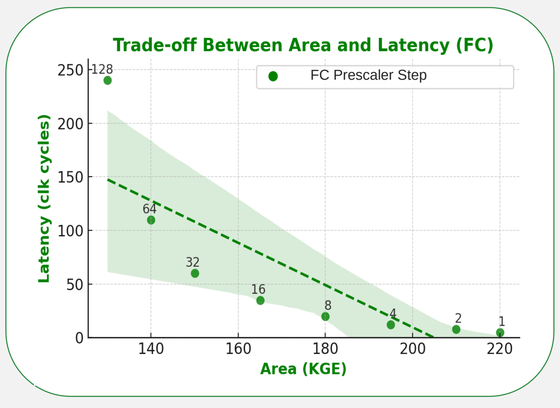
- We set up TMU on Cheshire[1] platform to monitor transactions passing through Ethernet IP[2].



- We synthesized TMU in GF12 technology under four configurations: FC and TC, with and without prescaler.







4 Conclusion

- TMU enhances AXI4 reliability with real-time fault detection and recovery.
- Two variants (FC & TC) offer a trade-off between tracking granularity and area efficiency.
- Validated at IP & system levels, ensuring low overhead and robust fault detection.

References

1. A. Ottaviano et al., "Cheshire: A Lightweight, Linux-Capable RISC-V Host Platform for Domain-Specific Accelerator Plug-In," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 10, pp. 3777-3781, Oct. 2023,
2. C. Liang et al.," A Gigabit, DMA-enhanced Open-Source Ethernet Controller for Mixed-Criticality Systems". In Proceedings of the 21st ACM International Conference on Computing Frontiers: Workshops and Special Sessions (CF '24 Companion)
3. T. Benz et al., "AXI-REALM: A Lightweight and Modular Interconnect Extension for Traffic Regulation and Monitoring of Heterogeneous Real-Time SoCs", DATE, 2024

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