Fast End-to-End Simulation and Exploration of Many-RISCV-Core Baseband Transceivers for SDR-Access Networks

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Software-defined 6G-baseband

- Multi-vendor components → Open hardware&software
- More network functions at the edge → Distributed intelligence
- Diverse scenarios and evolving standards → **Software-Defined**

Modeling&Simulation Requirements

1. Deterministic behaviour
2. Flexibility to evolving standard
3. Awareness of Timing
4. Fast for Monte Carlo simulation

Banshee: Static Binary Translation based simulator for design-space exploration on **TeraPool**, a **1024-cores** RISC-V 6G BB-receiver

Python model

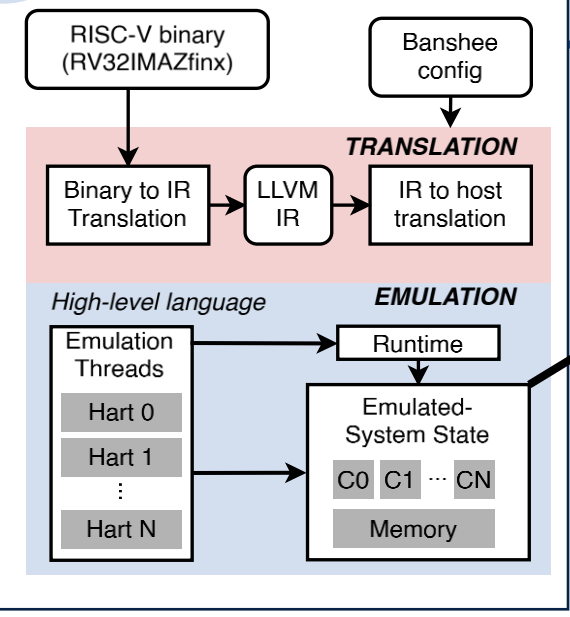
- Generate TX-data
- Map bits to QAM-symbol
- Simulate the wireless channel

LLVM 12.0

Compile RISC-V Binary

mmse.c | runtime.c | main.c

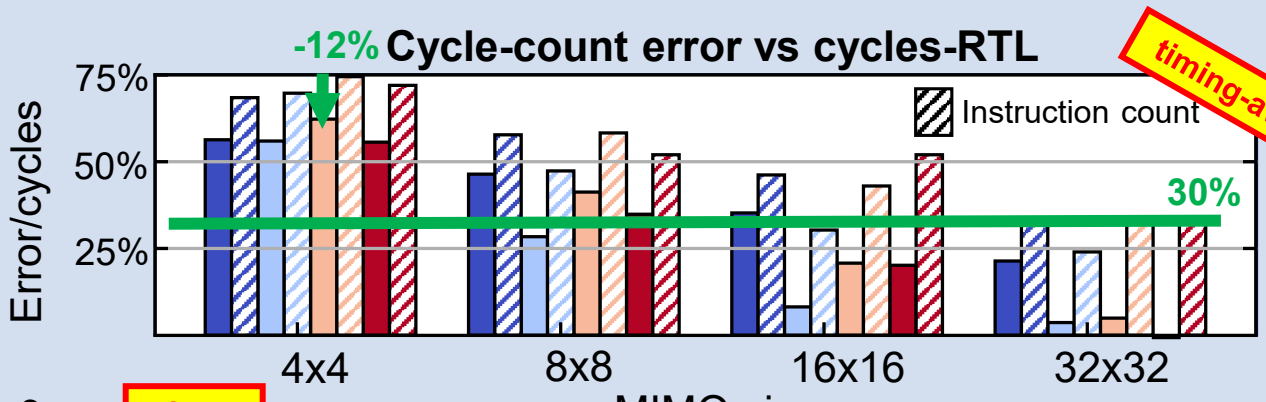
Banshee

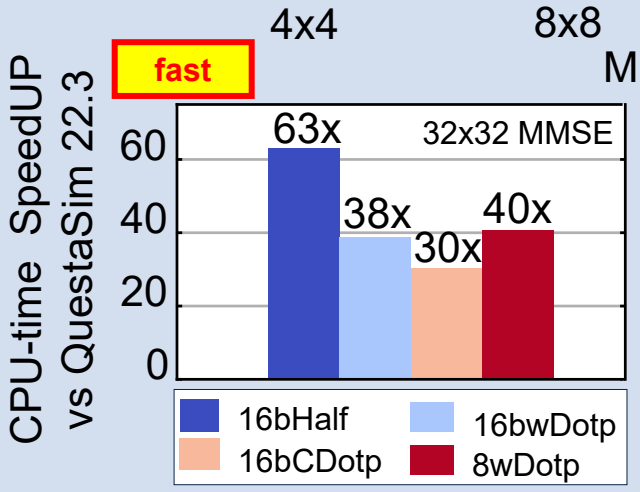


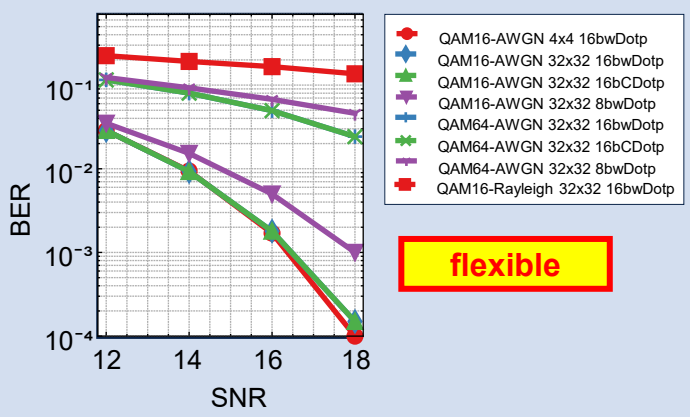
Python model

- Map QAM-symbol to bits
- Evaluate metrics (e.g. BER)

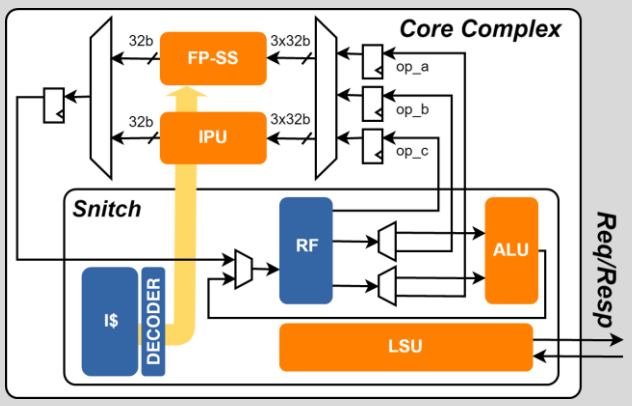
- Less than **30%** average cycle-count error, **12%** smaller than instr.-count
- **Parallel NxM MMSE: 63x** faster than Questasim 22.3, **< 2m:45s** wall-clk time
- **Single-Snitch 1638-subcarriers MC-itr:**
  9.44s/itr (4x4 MMSE) **3min/itr** (32x32 MMSE)



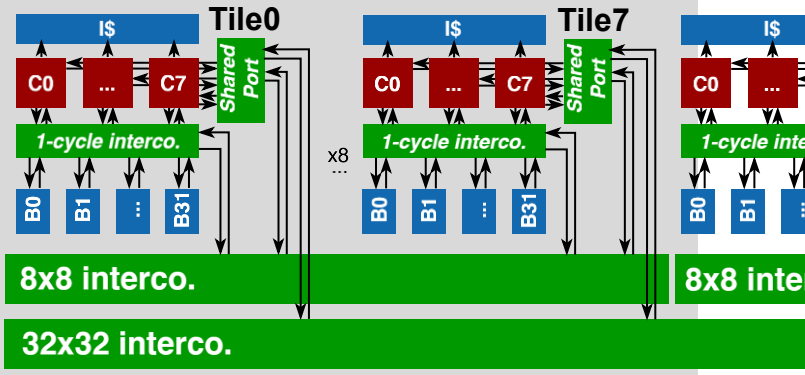




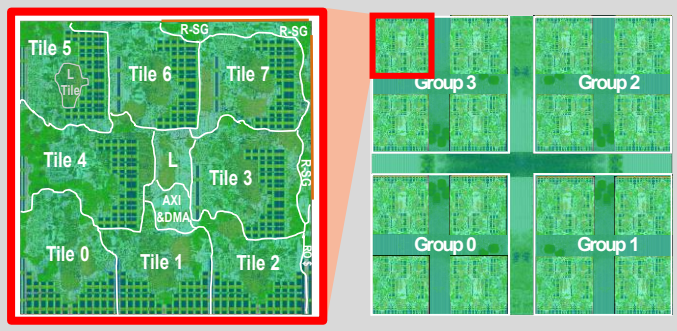
1. 1024 lightweigth **Snitch** cores, RISCV32IMA + **BB-processing ISA**



2. Hierarchical interconnect



3. Physically feasible



GF12 910MHz @25°C,0.8V

github.com/pulp-platform/mempool github.com/pulp-platform/banshee