Dual-Issue Execution of Mixed Integer and Floating-Point Workloads on Energy-Efficient In-Order RISC-V Cores

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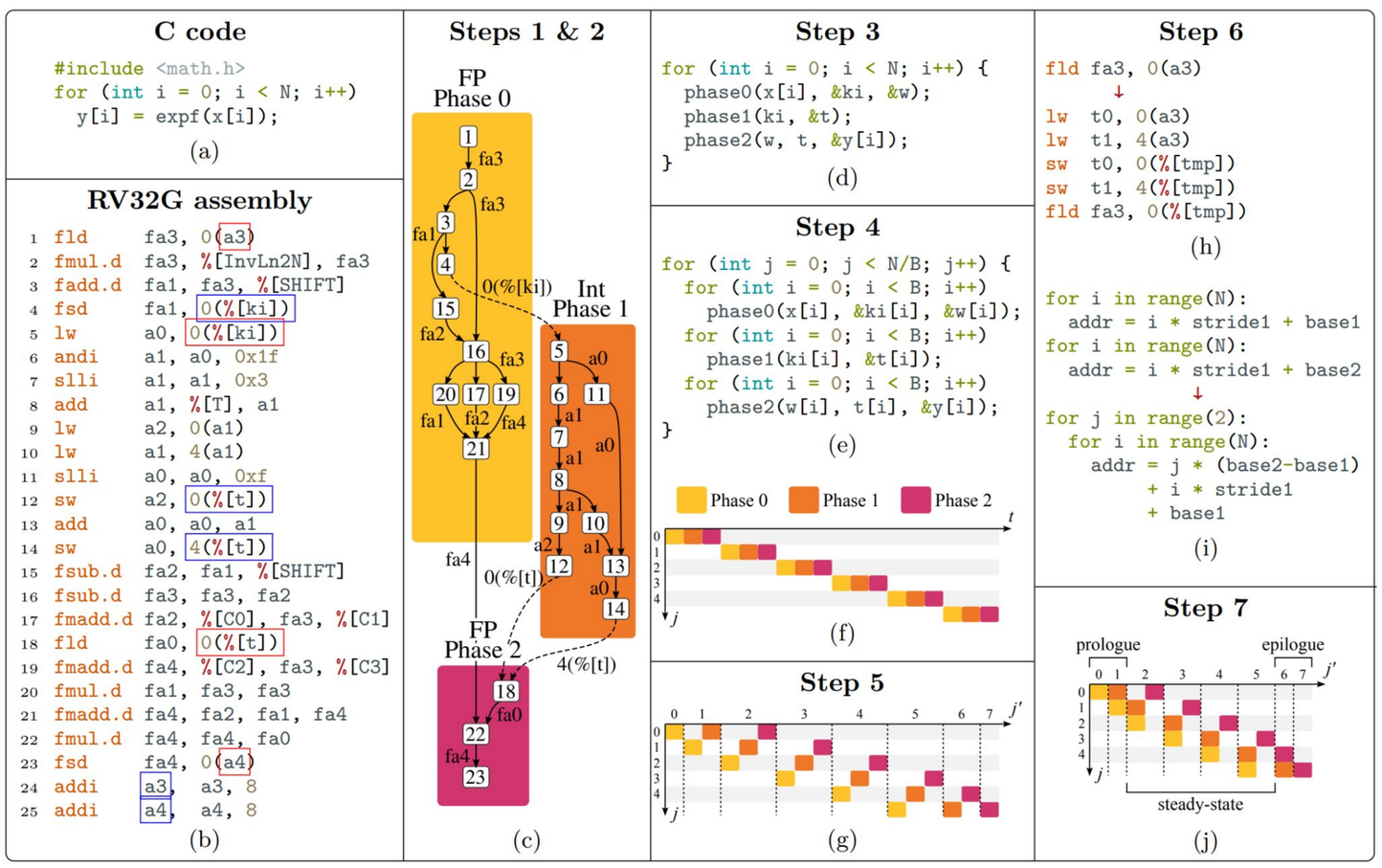
1 Introduction

To meet the **computational requirements** of modern workloads under **tight energy constraints**, general-purpose accelerator architectures have to integrate an ever-increasing number of area and **energy-efficient** PEs. In this context, **single-issue in-order** cores are commonplace, but lean dual-issue cores could boost PE IPC, especially for **mixed integer and floating-point** workloads. We present the **COPIFT methodology** and RISC-V **ISA extensions** to enable **low-cost** and flexible **dual-issue execution** of mixed integer and floating-point instruction sequences. We observe **1.47x speedup**, for a peak **1.75 IPC**, and **1.37x energy reduction** on average, over optimized RV32G baselines.

2 Implementation

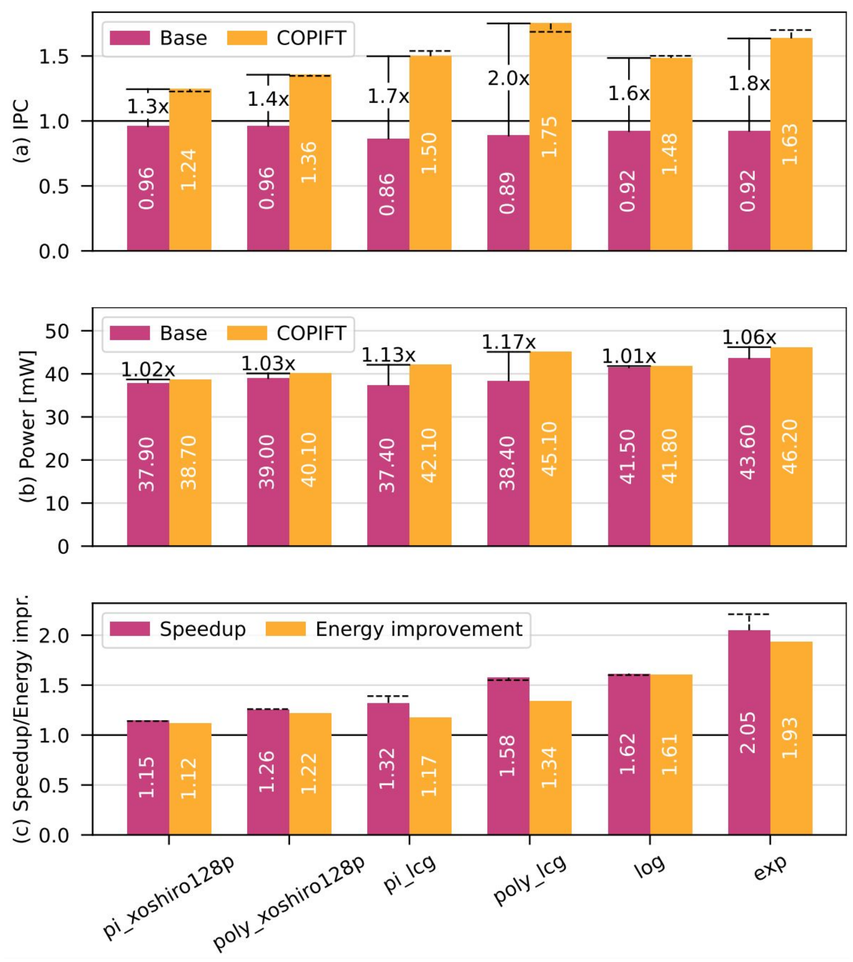
The following illustration depicts our COPIFT methodology applied to a sample mixed integer and floating-point kernel, calculating the exponential of a vector, as found e.g. in softmax layers.



Through the illustrated code transformations, we can overlap the integer and floating point thread executions, while preserving inter-thread dependencies, ensuring program correctness. Communication between the two threads occurs through the tightly-coupled data memory, thanks to an existing ISA extension of the single-issue in-order Snitch core, namely Stream Semantic Registers (SSRs).

3 Results

On a Snitch cluster implemented in GF12LP+ FinFET technology, at a target clock frequency of 1 GHz, our ISA extensions introduce **negligible area and timing overheads**, within the margin of synthesis process variability.



We evaluate our implementation on a variety of mixed integer and floating point workloads, measuring **1.47x speedup** on average, a peak **IPC of 1.75**, and an average **1.37x energy reduction**, over optimized RV32G baselines.

4 Conclusion

We presented COPIFT, a generic methodology to enable sustained dual-issue execution of mixed integer and floating-point instruction sequences in area and energy-efficient cores, validating our methodology and ISA extensions in Snitch, a state-of-the-art open-source RISC-V processor.

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PULP Parallel Ultra Low Power