DAC Young Fellows

DESIGN AUTOMATION CONFERENCE 58
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An FPGA-based Hardware-In-The-Loop co-design for Real-Time Power and Thermal Management emulation

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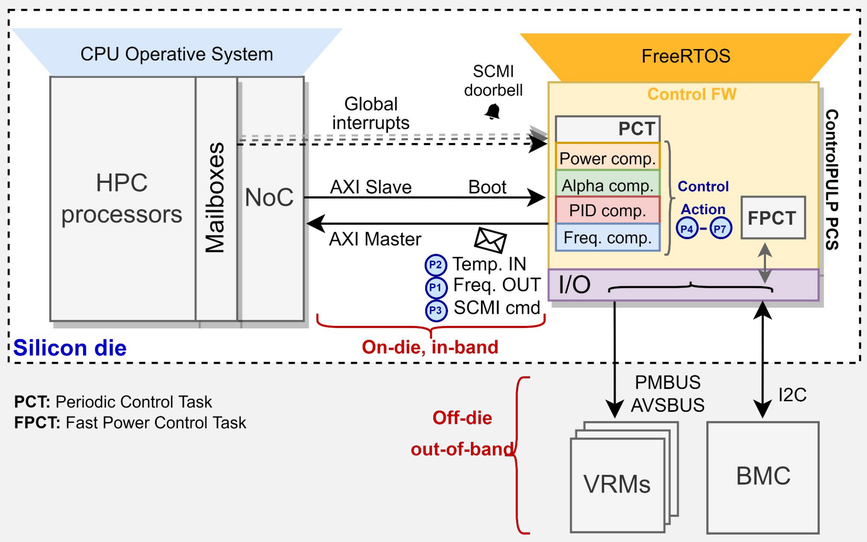
1 Leveraging Heterogeneous processing for Power and Thermal management emulation

- Pure software or commercial monolithic HIL solutions for real-time systems simulation **are often insufficient**
- Recent **FPGA-based heterogeneous SoCs** guarantee **rapid and cycle accurate prototyping** by combining soft IPs in advanced technology nodes with FPGA programmable logic
- We exploit this concept and build an FPGA-based HIL around a **RISC-V power controller for HPC processors**, ControlPULP

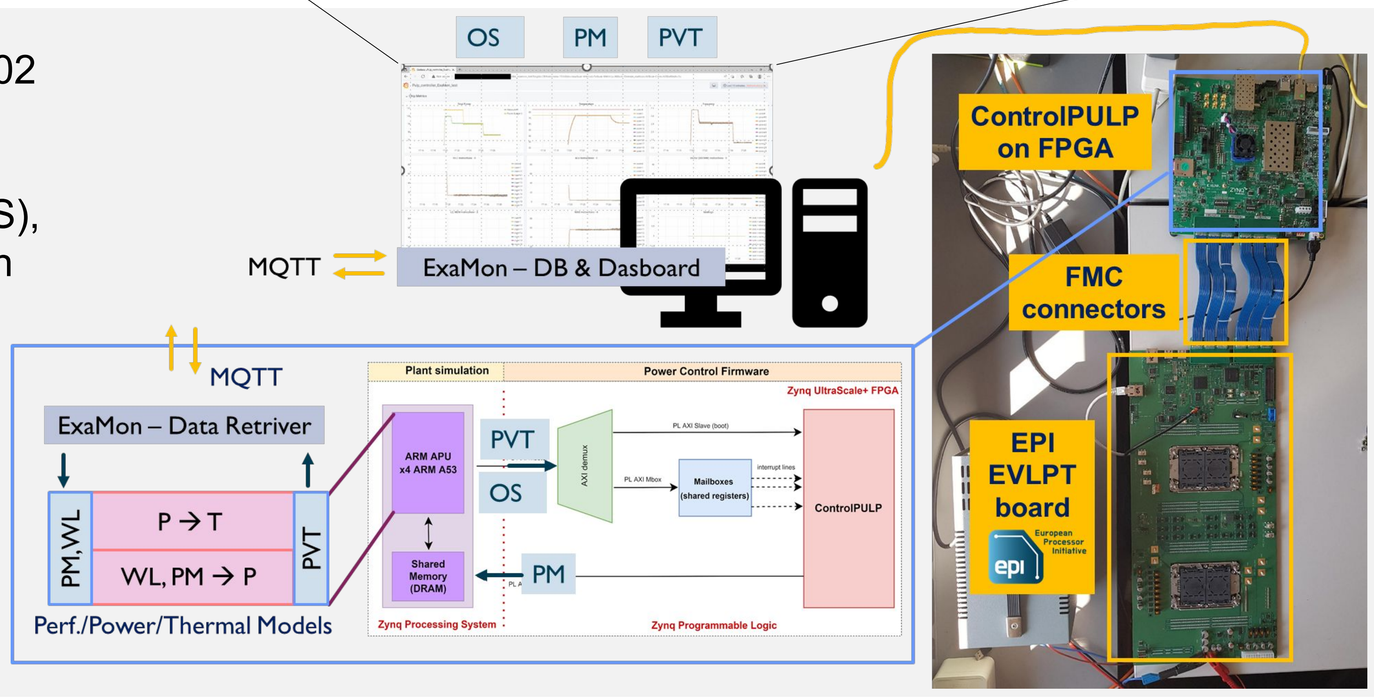
2 ControlPULP platform



- **First open-source (HW/SW) parallel power controller** in the RISC-V ecosystem[1]
- Executes **reactive**, PID-based hierarchical control on top of **FreeRTOS**[2]

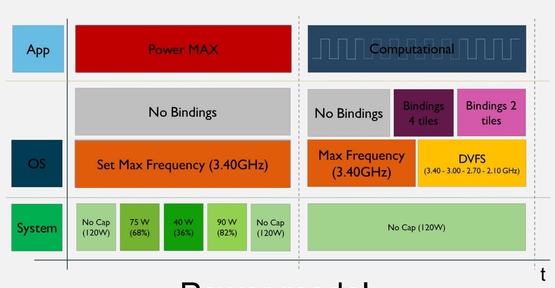
3 FPGA-HIL co-design

- ControlPULP mapped on Xilinx Ultrascale+ ZCU102 as Programmable Logic (PL).
- **Closed loop** with ZCU102 Processing System (PS), i.e. 4 ARMv8 Cortex-A53 cores, and **ExaMon²** with real-time monitoring dashboards
- 4 GiB DDR4 DRAM as shared memory.
- **Plant simulation** is three-fold:
  - Power and Thermal **capping**
  - Workload adaptation
  - OS interaction and **setpoint tracking**

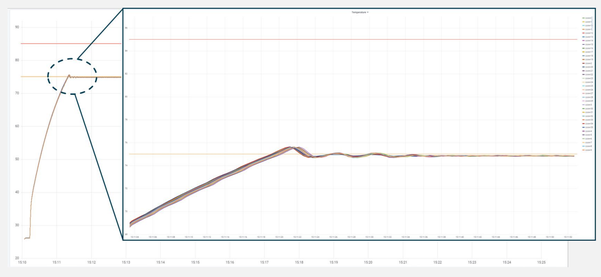


4 Evaluation

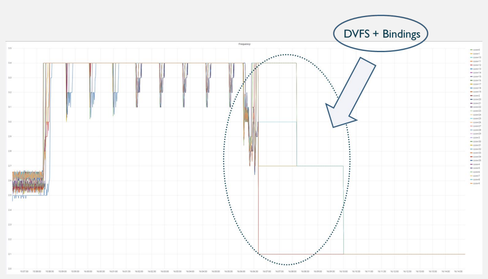
The emulation framework enables **real-time setpoint tracking** under power budget constraints.



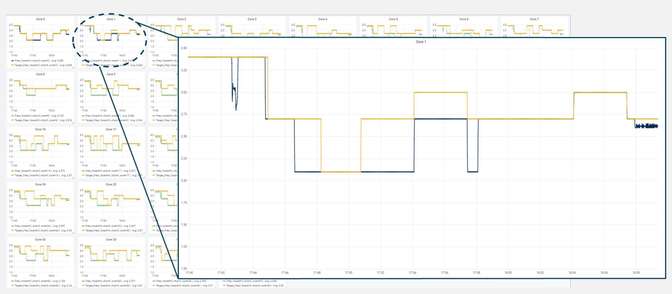
Power model



Thermal capping



DVFS + bindings



Per-core real-time frequency tracking

5 Conclusion

- FPGA-HIL emulation allows real-time, cycle-accurate and flexible prototyping and verification of control systems
- Check the demo presented at HiPEAC 2022 by **scanning the QR code** on the right!

[1] A. Ottaviano *et al.*, "ControlPULP: A RISC-V Power Controller for HPC Processors with Parallel Control-Law Computation Acceleration", 2022.
[2] G. Bambini *et al.*, "An Open-Source Scalable Thermal and Power Controller for HPC Processors," 2020.
[3] https://github.com/EEESlab/examon