PULP Project Update

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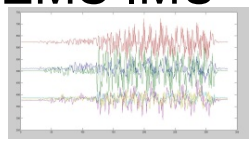
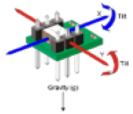
Computing fot the Internet of Things

Sense

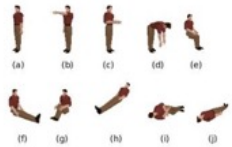
MEMS IMU



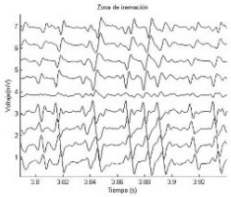


MEMS Microphone

ULP Imager



EMG/ECG/EIT



100 µW ÷ 2 mW

Analyze and Classify

µController

e.g. CortexM

IOs

1 ÷ 10 mW

Battery + Harvesting powered → a few mW power envelope

Transmit

Short range, medium BW

Low rate (periodic) data

SW update, commands

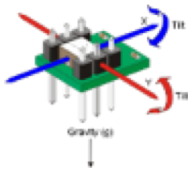
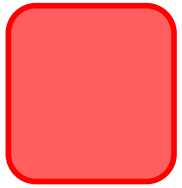
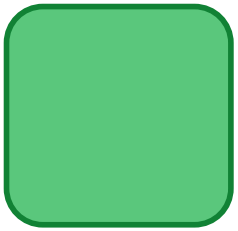
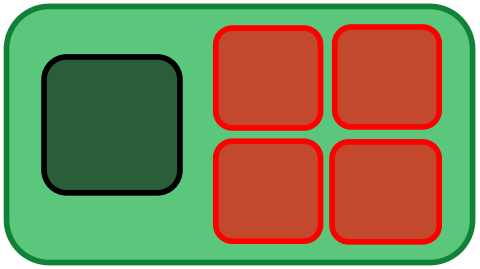
Long range, low BW

LoRa SEMTECH

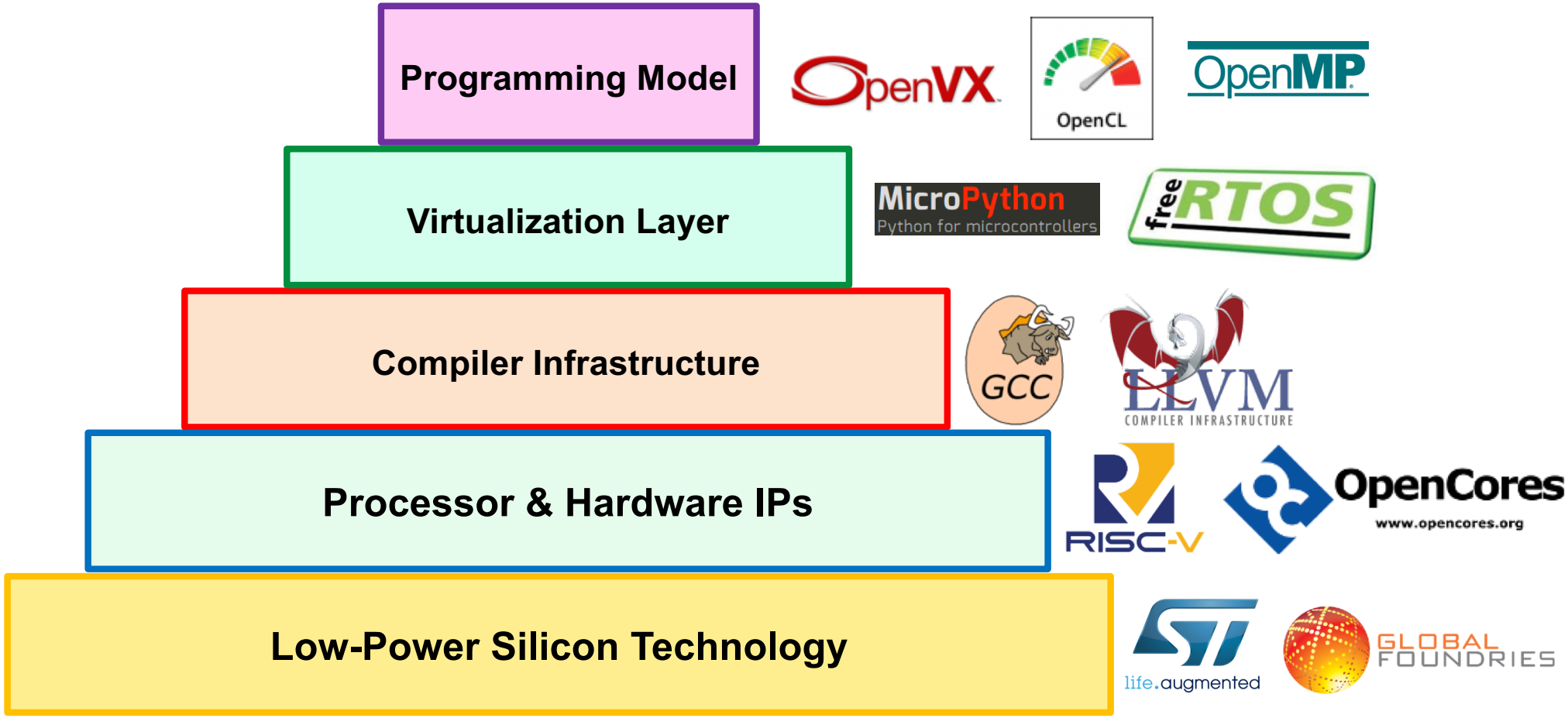
Idle: ~1µW
Active: ~ 50mW

PULP

Which Computing Platform?

SENSOR BANDWIDTH	COMPUTATIONAL DEMAND	COMPUTING PLATFORM
 ~ 1 bps	<1 MOPS	 *e.g. CortexM0*
 ~1 Kbps	~10 MOPS	 *e.g. CortexM3*
 ~100 Kbps	~ 100 MOPS	 *e.g. CortexM4/M4F*
 ~1000 Kbps	~ 1000 MOPS	 ?

PULP: Parallel Computing For The IoT



The output of our research on PULP is open source (Solderpad License)

PULP

PULP Open-Source Releases and External Contributions

Releases

1. **February 2016**
   First release of **PULPino**, our single-core microcontroller
2. **May 2016**
   Toolchain and compiler for our RISC-V implementation (**RI5CY**), DSP extensions
3. **August 2017**
   PULPino updates, new cores Zero-riscy and Micro-riscy, FPU, toolchain updates
4. **February 2018**
   PULPissimo, ARIANE
5. **March 2018**
   Open PULP, SDK, VP
5. **September 2018**
   Multi-Cluster PULP: Hero

Community Contributions

1. **June 2017**
   Porting of **Verilator and BEEBS** benchmarks to PULPino
   https://github.com/embecosm/ri5cy
2. **September 2017**
   Porting of **ARM CMSIS** to PULPino
   https://github.com/misaleh/CMSIS-DSP-PULPino
3. **November 2017**
   Numerous **Bug fixes** to RI5CY in PULPino
   https://github.com/pulp-platform/riscv
4. **December 2017**
   STING: Open-Source Verification Environment for PULPino
   http://valtrix.in/programming/running-sting-on-pulpino

PULP

The PULP family explained

RISC-V Cores

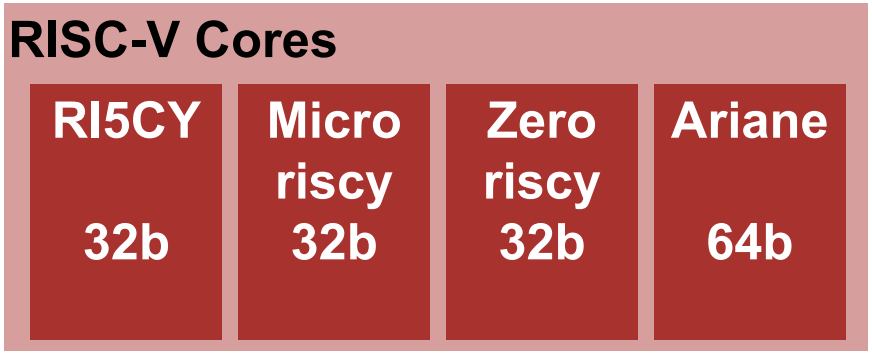
Peripherals

Interconnect

Platforms

Accelerators

We have developed several optimized RISC-V cores



Our RISC-V cores

32 bit

Low Cost Core

- **Zero-riscy**
  - RV32-ICM
- **Micro-riscy**
  - RV32-CE

ARM Cortex-M0+

Core with DSP enhancements

- **RI5CY**
  - RV32-ICMX
    - SIMD
    - HW loops
    - Bit manipulation
    - Fixed point

ARM Cortex-M4

Floating-point capable Core

- **RI5CY+FPU**
  - RV32-ICMFX

ARM Cortex-M4F

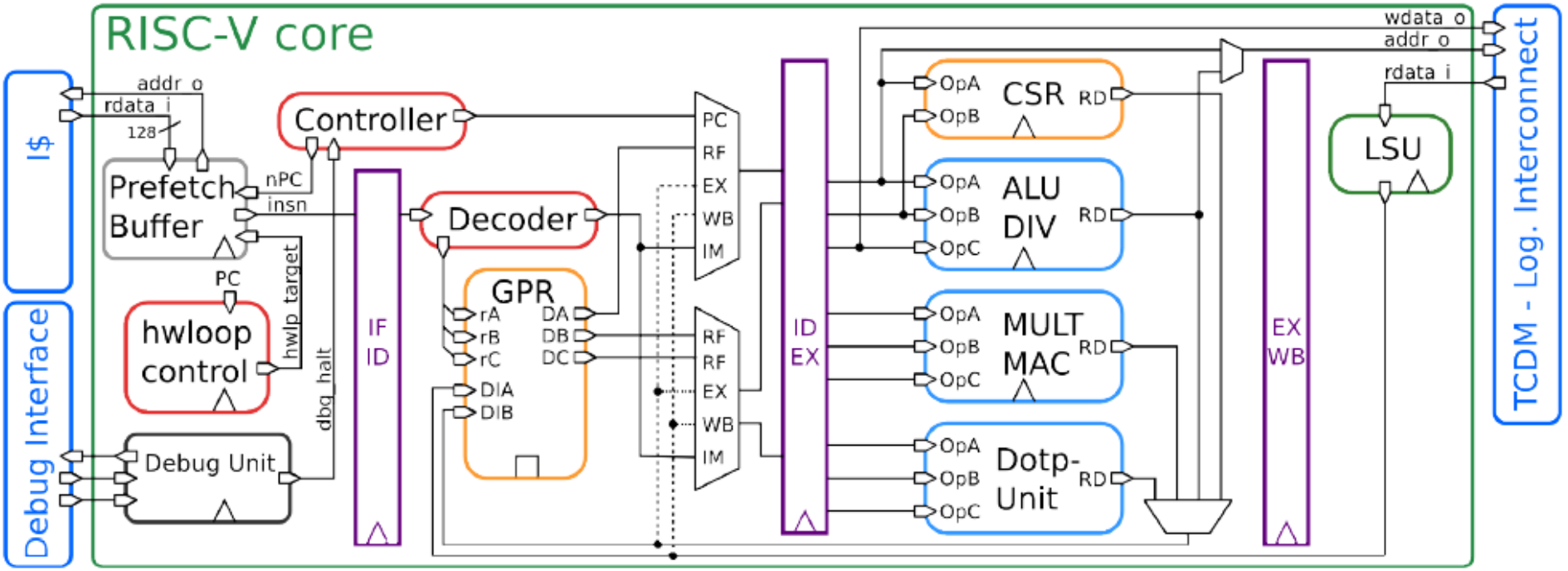
64 bit

Linux capable Core

- **Ariane**
  - RV64-ICM

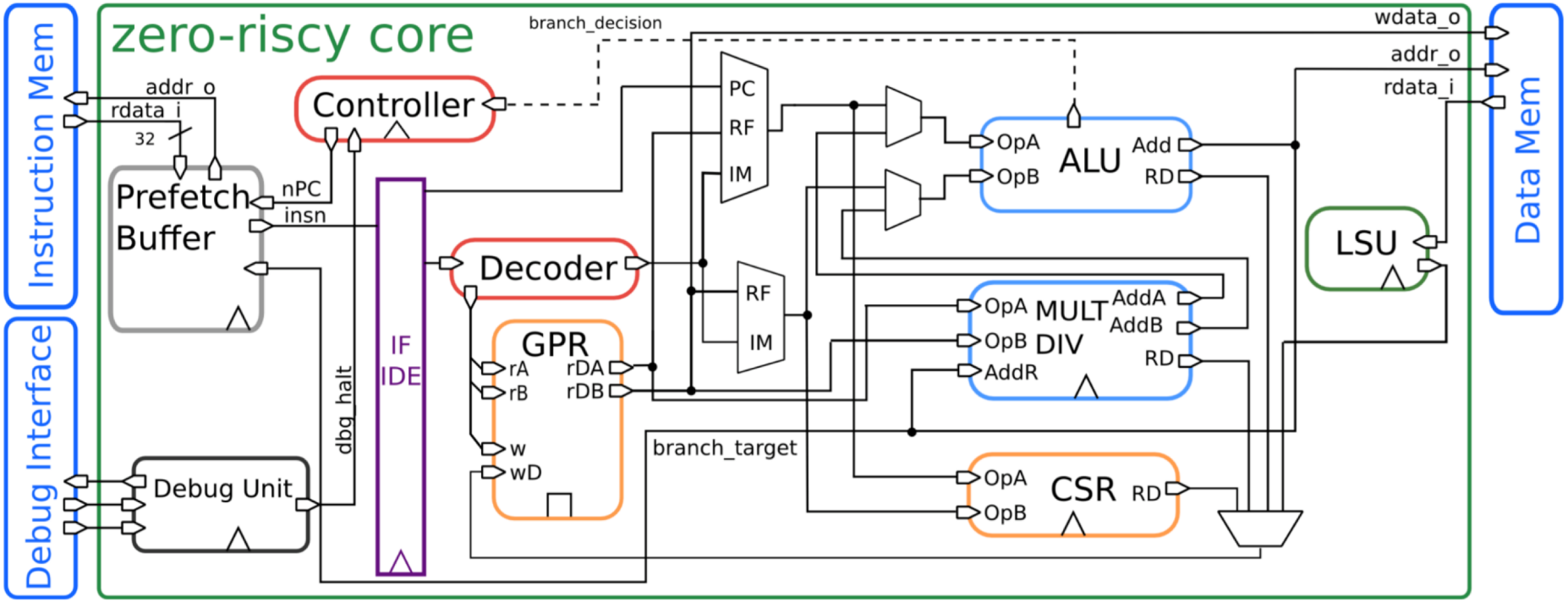
ARM Cortex-A55

RI5CY – Our workhorse 32-bit core



- 4-stage pipeline, optimized for energy efficiency
- 40 kGE, 30 logic levels, Coremark/MHZ 3.19
- Includes various extensions (X) to RISC-V for DSP applications

Zero/Micro-riscy, small area core for control applications

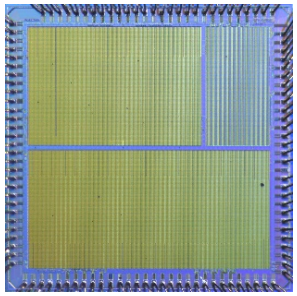


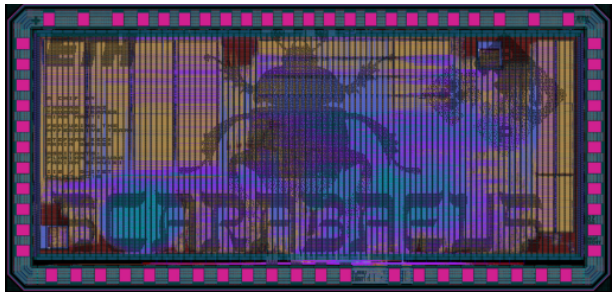
- Only 2-stage pipeline, simplified register file
- **Zero-Riscy** (RV32-ICM), 19kGE, 2.44 Coremark/MHz
- **Micro-Riscy** (RV32-EC), 12kGE, 0.91 Coremark/MHz
- Used as SoC level controller in newer PULP systems

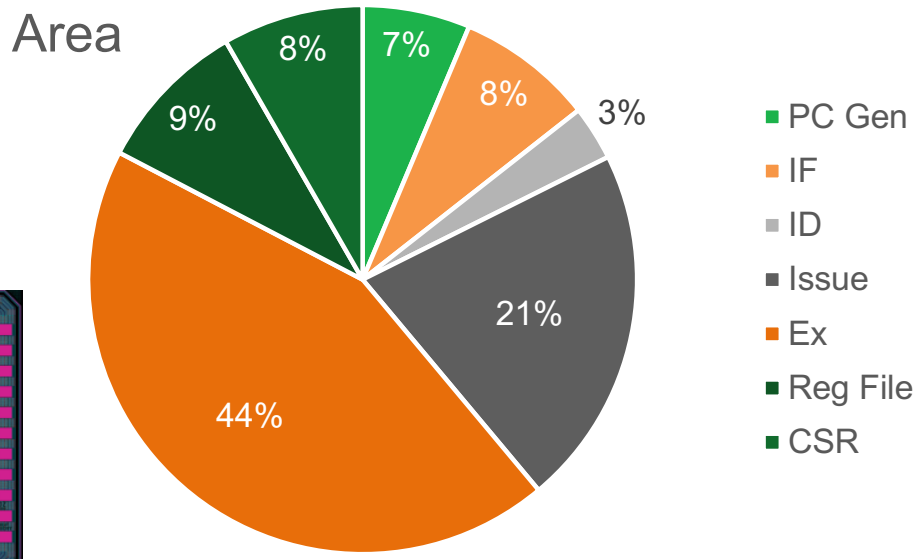
PULP

ARIANE: Our Linux Capable 64-bit core

- Tuned for high frequency, 6 stage pipeline, integrated cache
  - In order issue, out-of-order write-back, in-order-commit
  - Supports privilege spec 1.11, M, S and U modes
  - Hardware Page Table Walker
- Implemented in GF22nm (Poseidon), and UMC65 (Scarabaeus)
  - In 22nm: 910 MHz worst case conditions (SSG, 125/-40C, 0.72V)
  - 8-way 32kByte Data cache and 4-way 32kByte Instruction Cache
  - Core area: 175 kGE



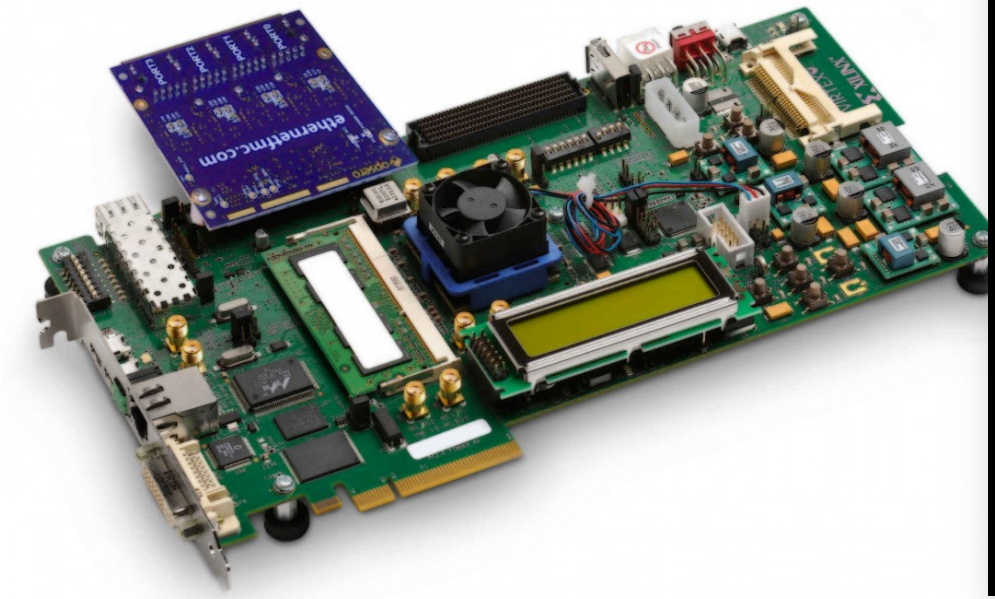




PULP

Ariane mapped to FPGA boots Linux

- **Full FPGA implementation**
  - Xilinx Vertex 7 – VC707
  - **Core:** 50 – 100 MHz
  - **Core:** 15 kLUTs
  - 1 GB DDR3
- Mapping to simpler boards underway



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                                .yMMMMMMMMN+
                              .yMMMMMMMMMMMMN+`
                            .yMMMMMdooooosmMMMMN+`
                          -yMMMMMMMy +sss.-MMMMMMN+`
                        -hMMMMMMMMMy /ooo.-MMMMMMMMNo`
                      -hMMMMMMMMMMMy osssymMMMMMMMMMNo
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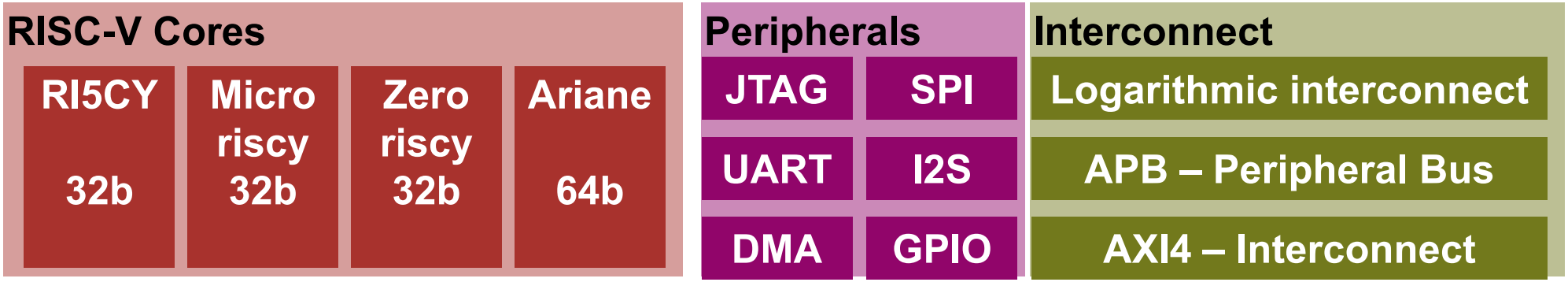
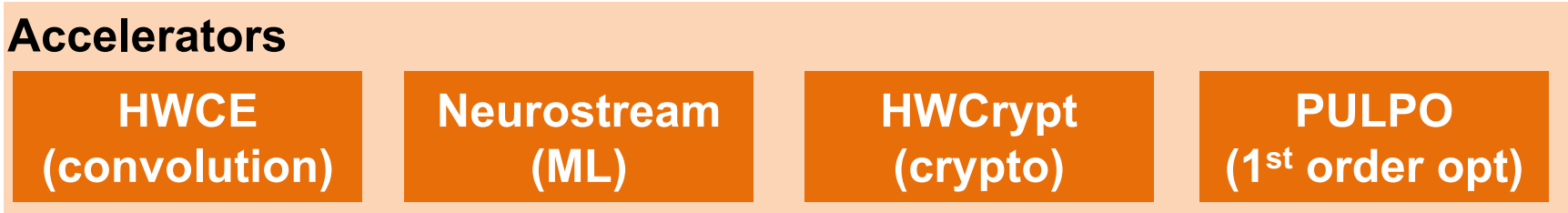
[    0.000000] OF: fdt: Ignoring memory range 0x80000000 - 0x80200000
[    0.000000] Linux version 4.12.3-00011-gb0e01a2-dirty (msc17f11@badile14.ee.ethz.ch) (gcc
 version 7.1.1 20170509 (GCC) ) #737 Fri Sep 8 11:03:09 CEST 2017
[    0.000000] Initial ramdisk at: 0xffffffff80014bd8 (534172 bytes)
[    0.000000] Built 1 zonelists in Zone order, mobility grouping off.  Total pages: 3535
[    0.000000] Kernel command line: console=sbi_console
[    0.000000] PID hash table entries: 64 (order: -3, 512 bytes)
[    0.000000] Dentry cache hash table entries: 2048 (order: 2, 16384 bytes)
[    0.000000] Inode-cache hash table entries: 1024 (order: 1, 8192 bytes)
[    0.000000] Sorting __ex_table...
[    0.000000] Memory: 11320K/14336K available (1484K kernel code, 105K rwdata, 305K rodata,
 608K init, 208K bss, 3016K reserved, 0K cma-reserved)
[    0.000000] SLUB: HWalign=64, Order=0-3, MinObjects=0, CPUs=1, Nodes=1
[    0.000000] NR_IRQS:32 nr_irqs:32 0
[    0.000000] riscv,cpu_intc,0: 64 local interrupts mapped
[    0.000000] clocksource: riscv_clocksource: mask: 0xffffffff max_cycles: 0xffffffff, max_
idle_ns: 76450417870 ns
```

PULP

Only processing cores are not enough, we need more





The pulp-platforms put everything together

RISC-V Cores

RI5CY	Micro riscy	Zero riscy	Ariane
32b	32b	32b	64b

Peripherals

JTAG	SPI
UART	I2S
DMA	GPIO

Interconnect

- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

Platforms

Single Core

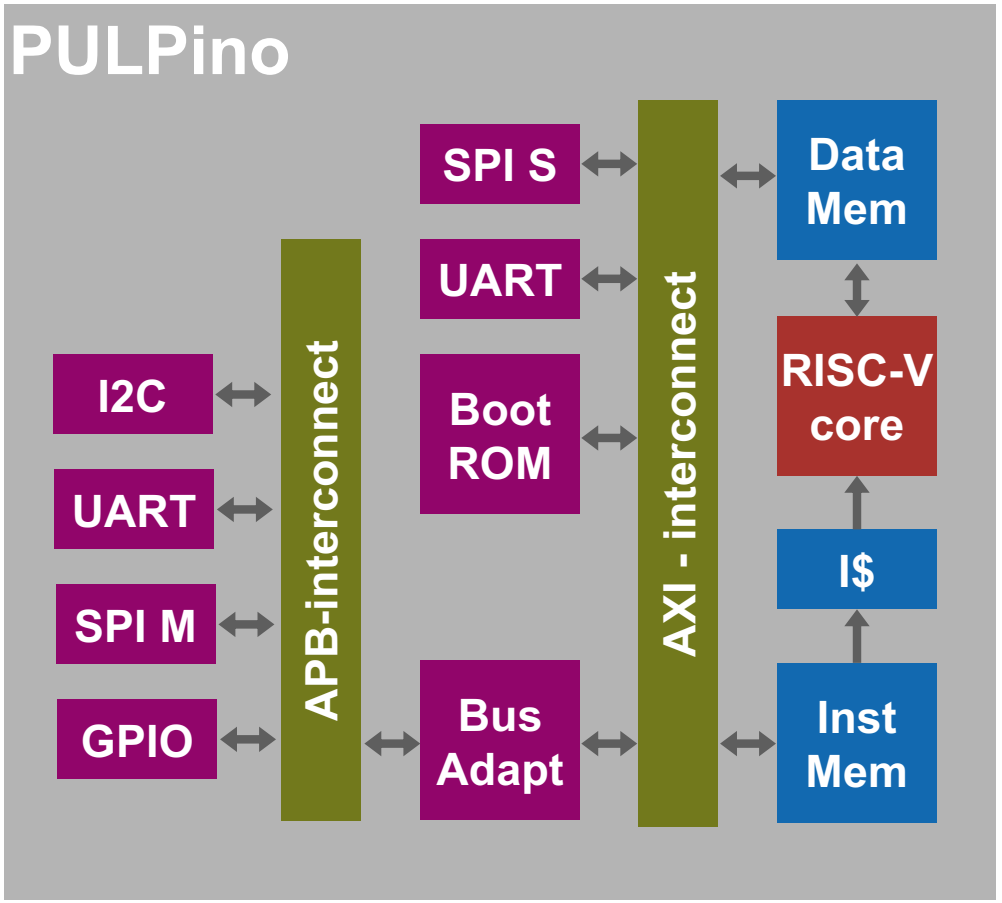
- PULPino
- PULPissimo
- Kerbin

Accelerators

- HWCE (convolution)
- Neurostream (ML)
- HWCrypt (crypto)
- PULPO (1st order opt)

PULPino our first single core platform

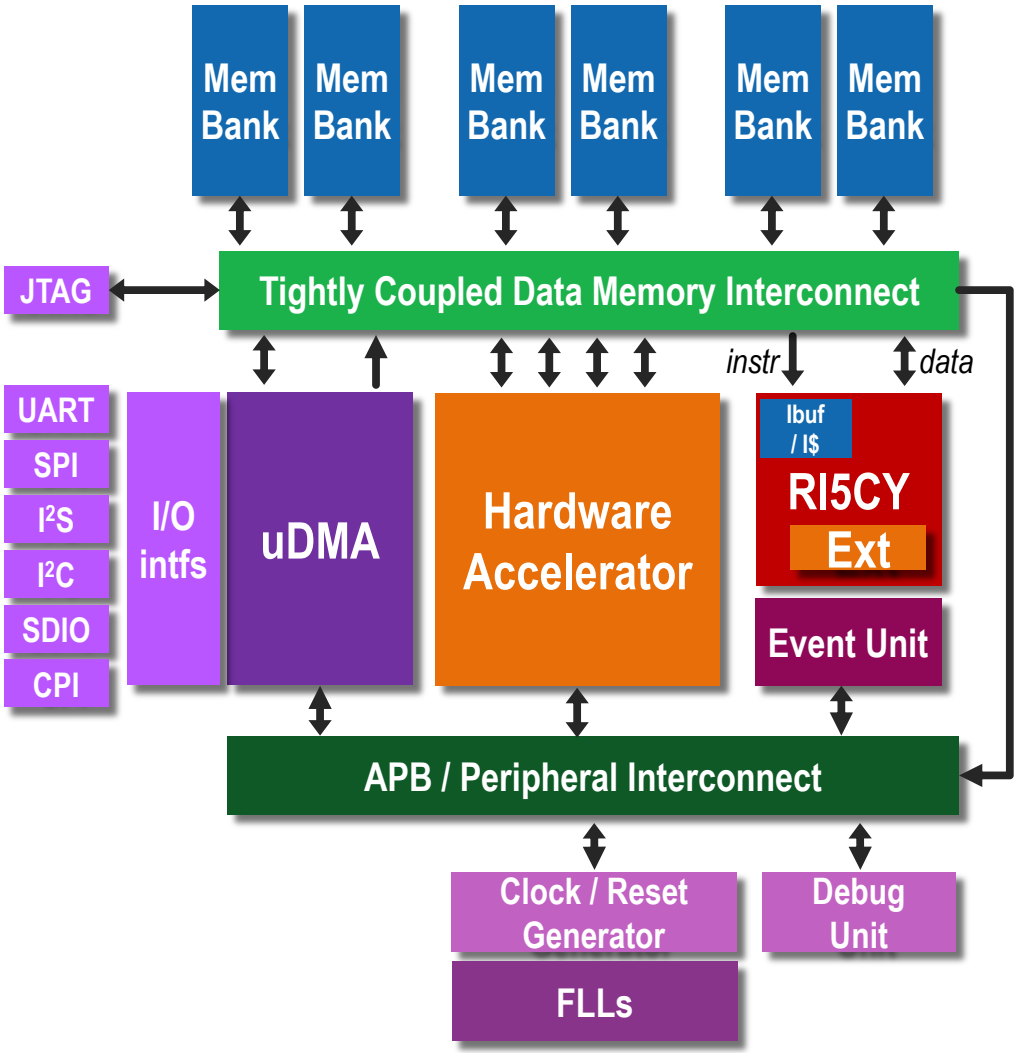
- **Simple design**
  - Meant as a quick release
- **Separate Data and Instruction memory**
  - Makes it easy in HW
  - Not meant as a Harvard arch.
- **Can be configured to work with all our 32bit cores**
  - RI5CY, Zero/Micro-Riscy
- **Peripherals copied from its larger brothers**
  - Any AXI and APB peripherals could be used



PULP

PULPissimo the improved single core platform

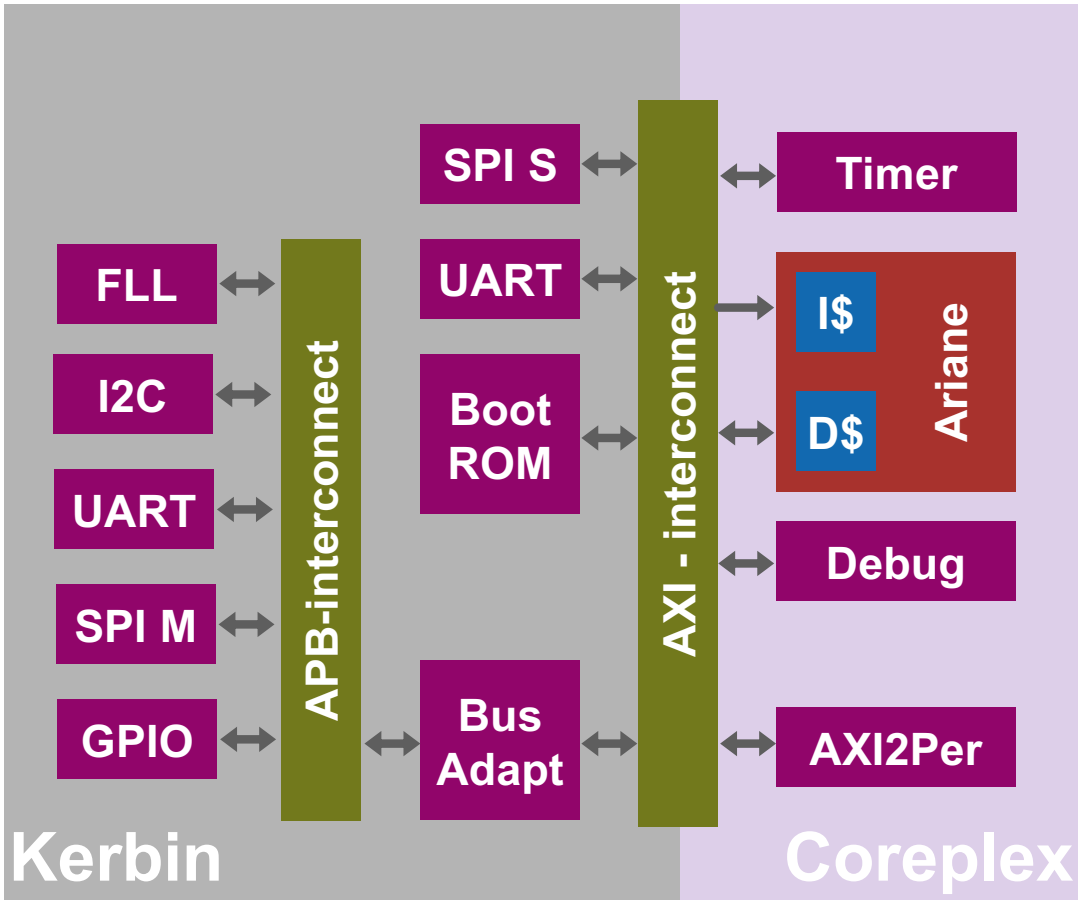
- **Shared memory**
  - Unified Data/Instruction Memory
  - Uses the multi-core infrastructure
- **uDMA for I/O subsystem**
  - Can copy data directly from I/O to memory without involving the core
- **Support for Accelerators**
  - Direct shared memory access
  - Programmed through APB bus
  - Number of TCDM access ports determines max. throughput
- **Used as a fabric controller in larger PULP systems**



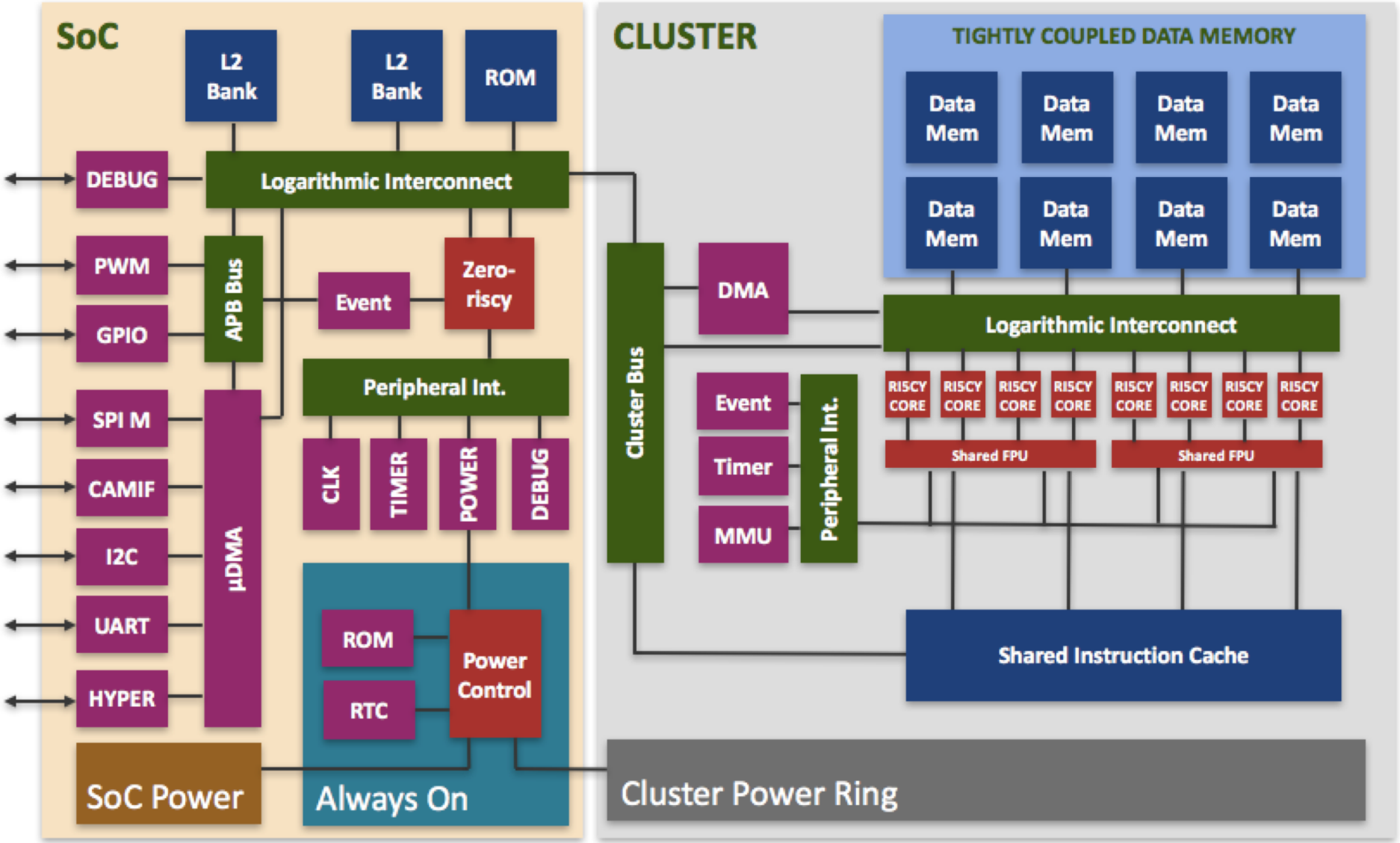
PULP

Kerbin the single core support structure for Ariane

- **Still work in progress**
  - Current version is very simple
  - Useful for in-house testing
  - A more advanced version will likely be developed soon.



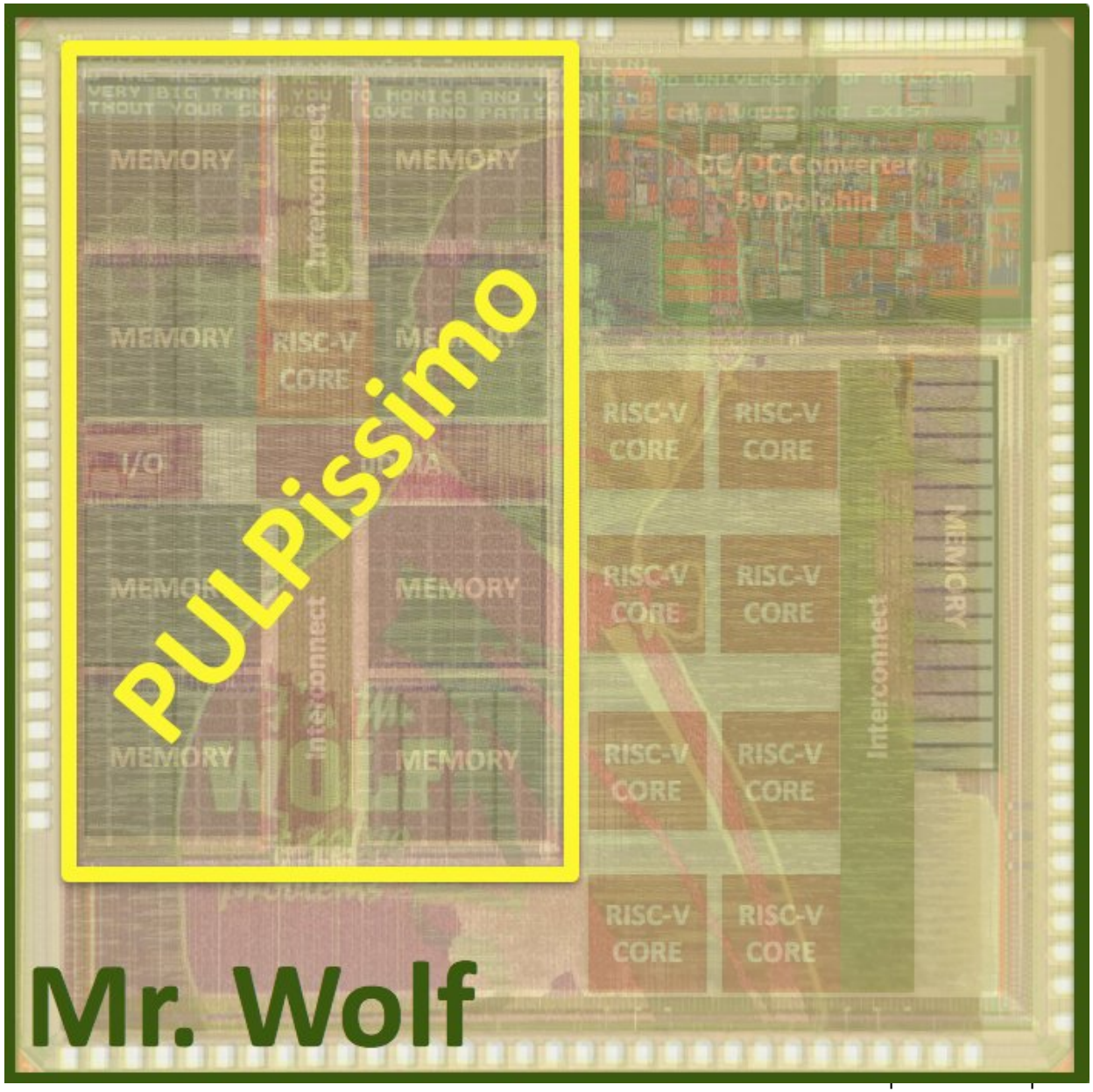
PULP in the IoT domain: Latest version Mr. Wolf



PULP

Mr. Wolf will (hopefully) solve problems

- TSMC 40LP - 9mm^2
- 64 pin QFN package
- Cluster with
  - 8x RI5CY
  - 2x shared FPUs
  - 64 kByte TCDM
- SoC domain with
  - micro-riscy core to control power modes
  - DC-DC converter (Dolphin) to regulate power
  - 512 kBytes L2

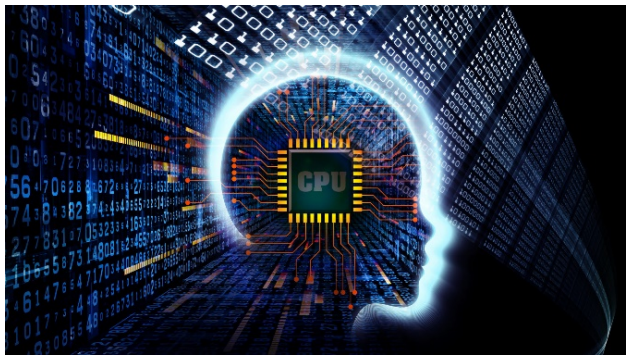


PULP

GAP8: PULP-Based Industry IoT processor

- GAP-8 processor:
  - 8-cores PULP system
  - Neural network based pattern matching engine
  - Up to 8 GOPS, 300 MOPS for 1mW
- Commercialized by **GreenWaves Technologies** French Startup
- Developed in collaboration with University of Bologna and ETH Zurich
- GAPUINO evaluation boards available: www.greenwaves-technologies.com

Applications



Image, sound and vibrations pattern matching at unmatched power efficiency for the smart IoT

GreenOFDM: Disruptive low power OFDM wireless communication for the smart IoT

SW Defined Modem for any IoT wireless communication

PULP

Finally for HPC applications we have multi-cluster systems

RISC-V Cores

- RI5CY 32b
- Micro riscy 32b
- Zero riscy 32b
- Ariane 64b

Peripherals

- JTAG
- SPI
- UART
- I2S
- DMA
- GPIO

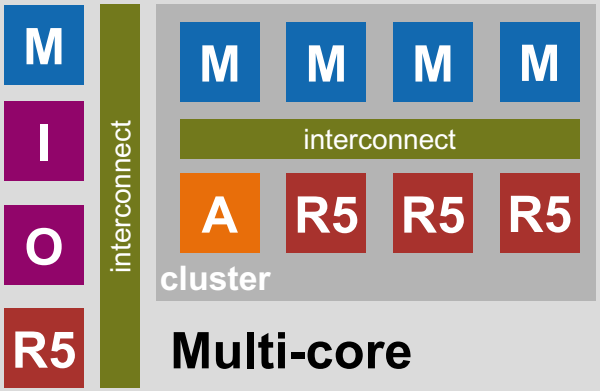
Interconnect

- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

Platforms

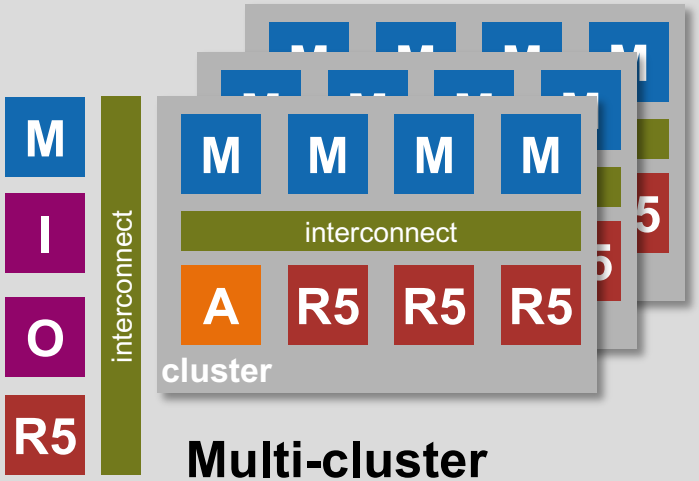
Single Core

- PULPino
- PULPissimo



Multi-core

- Fulmine
- Mr. Wolf



Multi-cluster

- Hero

IOT → HPC

Accelerators

- HWCE (convolution)
- Neurostream (ML)
- HWCrypt (crypto)
- PULPO (1st order opt)

Silicon and Open Hardware fuel PULP success

- **Many companies (we know of) are actively using PULP**
  - They value that it is **silicon proven**
  - They like that it uses a **permissive open source license**

Companies with announced products, business
Companies that use PULP internally or for training
Companies exploring opportunities

Companies that are using/evaluating PULP

- GreenWaves Technologies
- Dolphin
- IQ Analog (14nm chips)
- Embecosm
- lowRISC
- Mentor Graphics
- Cadence Design Systems
- ST Microelectronics (IT,F)
- Micron
- Google
- IBM
- NXP
- SIAE Microelectronica
- Advanced Circuit Pursuit
- Shanghai Xidian Technology
- SCS Zurich
- IMT technologies
- Microsemi
- Arduino
- RacyICs

Research Centers/Universities using PULP

- Stanford
- Cambridge
- UCLA
- CEA/LETI
- EPFL
- National Chia Tung University
- Politecnico di Milano
- Politecnico di Torino
- Universita Roma I
- Instituto Superior Tecnico – U. de Lisboa
- Fondazione Bruno Kessler
- Zagreb FER
- Universita di Genova
- Istanbul Technical U.
- RWTH Aachen
- Lund
- USI – Lugano
- Bar-Ilan
- TU-Kaiserslautern
- TU-Graz
- UC San Diego
- CSEM
- IBM Research

PULP

Thanks for your attention!!!

www.pulp-platform.org

pulp.ethz.ch
www-micrel.deis.unibo.it/pulp-project

https://twitter.com/pulp_platform

The fun is just beginning...

davide.rossi@unibo.it