**PULP PLATFORM**
Open Source Hardware, the way it should be!

# *Open Source HW and RISC-V*

*Linked, but not the same*

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**http://pulp-platform.org**

**@pulp_platform**

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# Open Source Hardware

**Hardware whose design is made publicly available so that anyone can study, modify, distribute, make, and sell the design or hardware based on that design**

(*source: Open Source Hardware (OSHW) Statement of Principles 1.0*)

Very wide definition – includes PCBs and “makers” stuff

**I will focus on Open Souce Computing Hardware (OSCHW)**

# OSCHW Needs an Open Source ISA

# Not only RISCV Cores – many IPs for a Platform

**RISC-V Cores**

- RI5CY 32b
- Ibex 32b
- Snitch 32b
- Ariane + Ara 64b

**Peripherals**

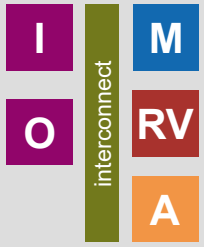
- JTAG
- SPI
- UART
- I2S
- DMA
- GPIO

**Interconnect**

- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

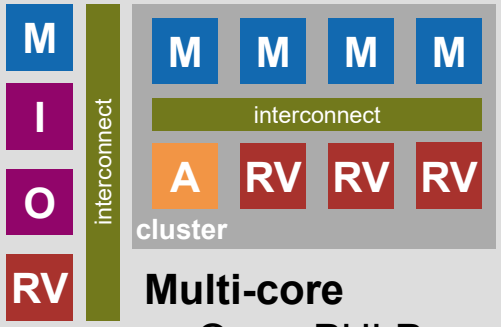
**Platforms**

https://github.com/pulp-platform/



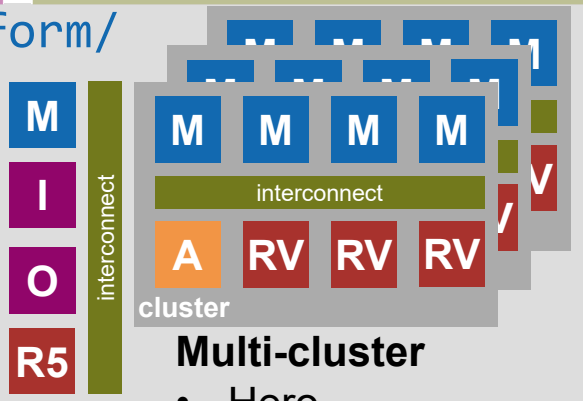

**Single Core**

- PULPino
- PULPissimo




**Multi-core**

- Open-PULP
- PULP-PM




**Multi-cluster**

- Hero
- Manticore

IOT → HPC

**Accelerators**

- HWCE (convolution)
- Neurostream (ML)
- HWCrypt (crypto)
- PULPO (1st ord. opt)

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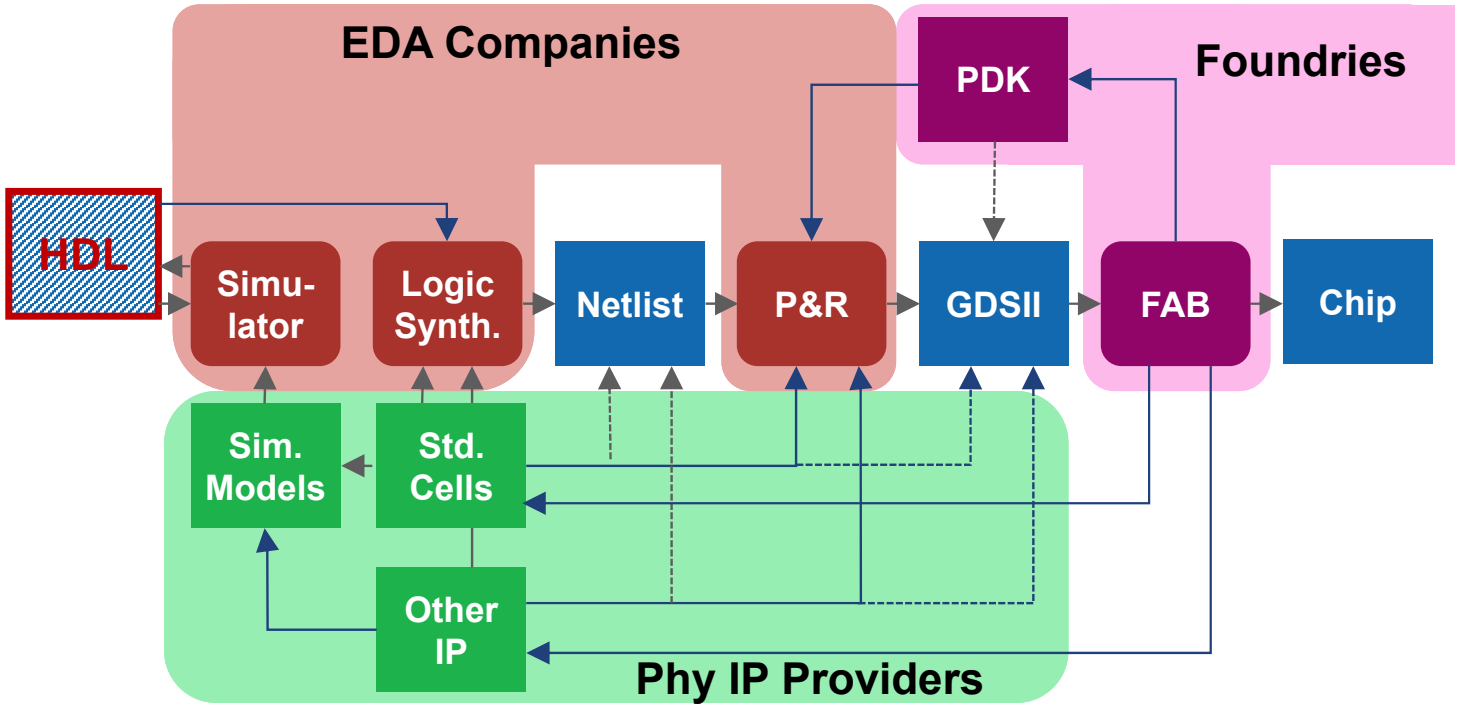
# Technically, what is “open” in OSCHW Today?

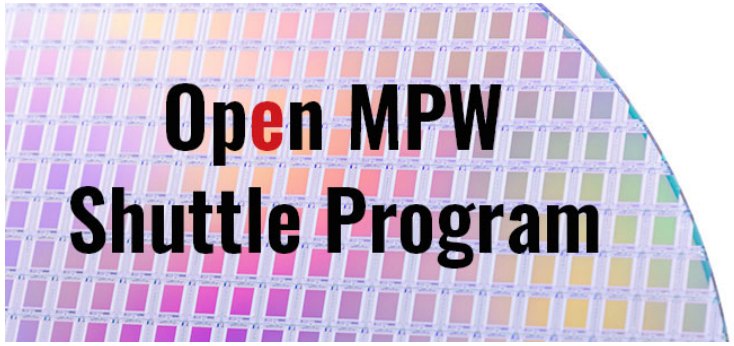
- **Only the first stage** of the silicon production pipeline
  → **RTL source code** (***permissive****, e.g. Apache is key for industrial adoption)
- Later stages contain closed IP of various actors → not open source by default




Cadence **license** for academic usage forbids ***permissive*** open sourcing of designs made with CDNS tools unless a ***reciprocal**** license is used

“See: https://cern-ohl.web.cern.ch/ (CERN-OHL-S, -W, -P)

# What about End-to-End Open HW (pdk, tools)?

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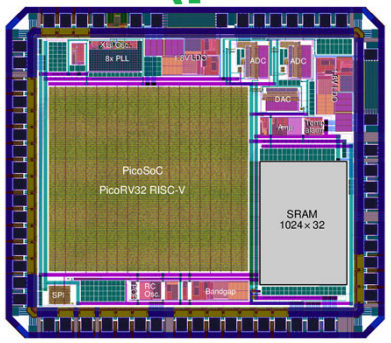


Raven 130nm mixed-signal SoC

**Open source process design kit** for usage with **SkyWater** Foundry 130nm tech.
https://github.com/google/skywater-pdk

**Open Source ASIC EDA flow**
**OpenLANE** is an automated RTL to GDSII flow based on several components including OpenROAD, Yosys, Magic, Netgen, Fault and custom methodology scripts for design exploration and optimization.
https://github.com/The-OpenROAD-Project/OpenLane

Can be done, but long-term investment & *not a prerequisite* for OSCHW. But we need at least non-proprietary design exchange standards and OSCHW friendly EDA licenses

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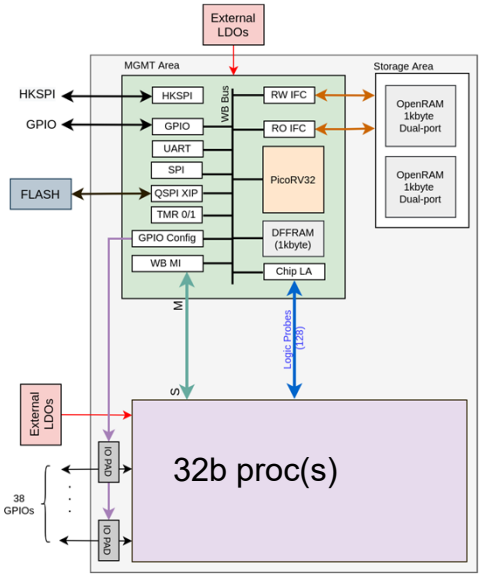
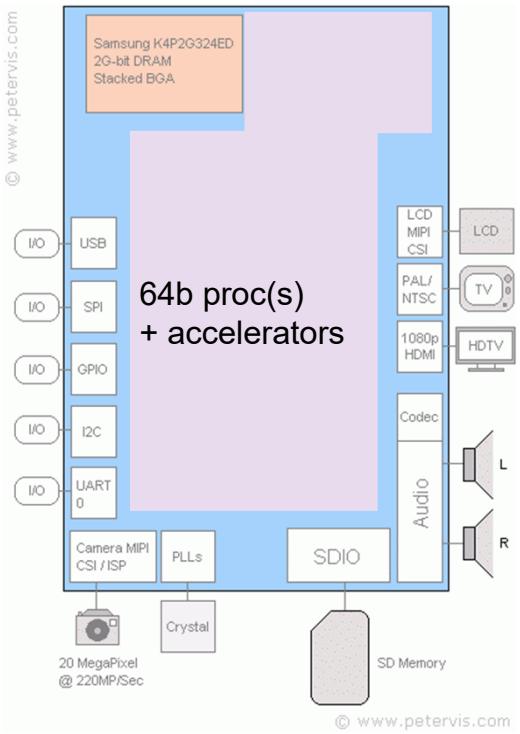
# Viable Short-term: SoC harness(es)

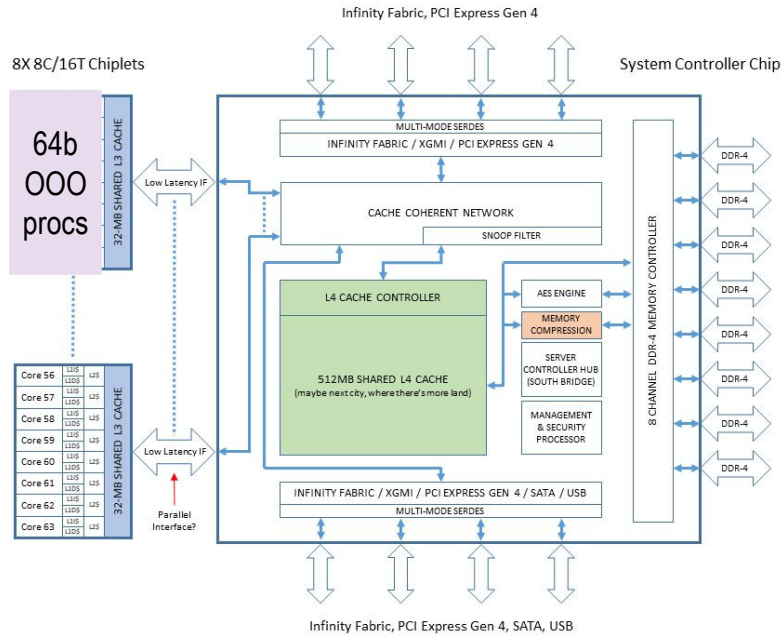
**MCU SoC Harness:** On-chip DC/DC, PLL, PM, NVM macro, MIPI-IO, PUF, EFUSE…

**APU SoC Harness:** same as MCU (higher perf) + LPDDR, Ethernet, HDMI phy (& CTRL)

**CPU SoC Harness:** DDR5, HBM, HBI, PCIe + 200G Ethernet, SATA, Other lower BW Phys




**Technology dependent Harness → closed, source, but standard and reusable**

# Scaling up OSCHW industrial ambition

**RISC-V Cores**

| RI5CY | Ibex | Snitch | Ariane + Ara |
|---|---|---|---|
| 32b | 32b | 32b | 64b |

**Peripherals**

| | |
|---|---|
| JTAG | SPI |
| UART | I2S |
| DMA | GPIO |

**Interconnect**

- Logarithmic interconnect
- APB – Peripheral Bus
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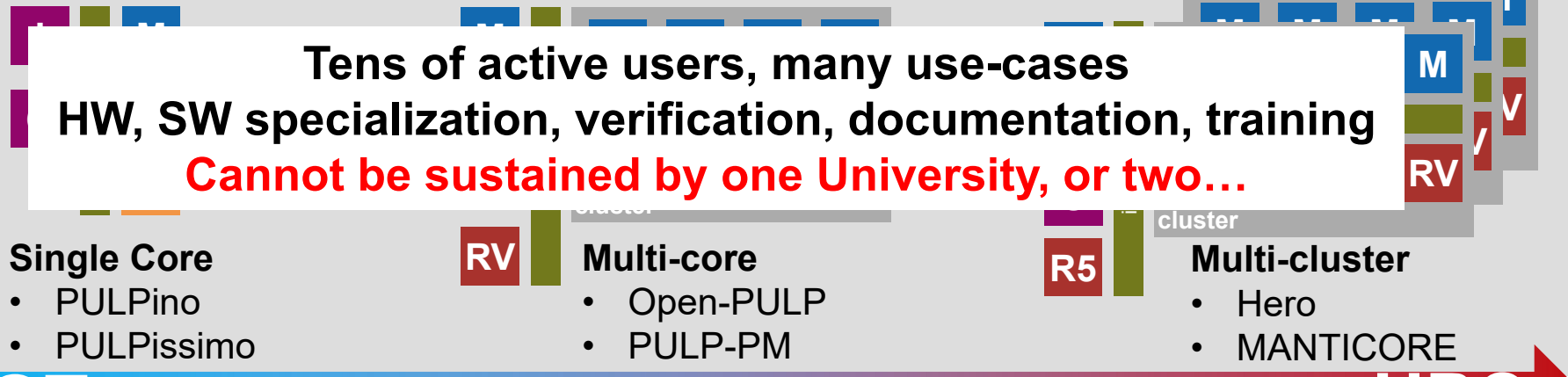
**Platforms**

**Tens of active users, many use-cases**
**HW, SW specialization, verification, documentation, training**
**Cannot be sustained by one University, or two…**

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|---|---|---|---|

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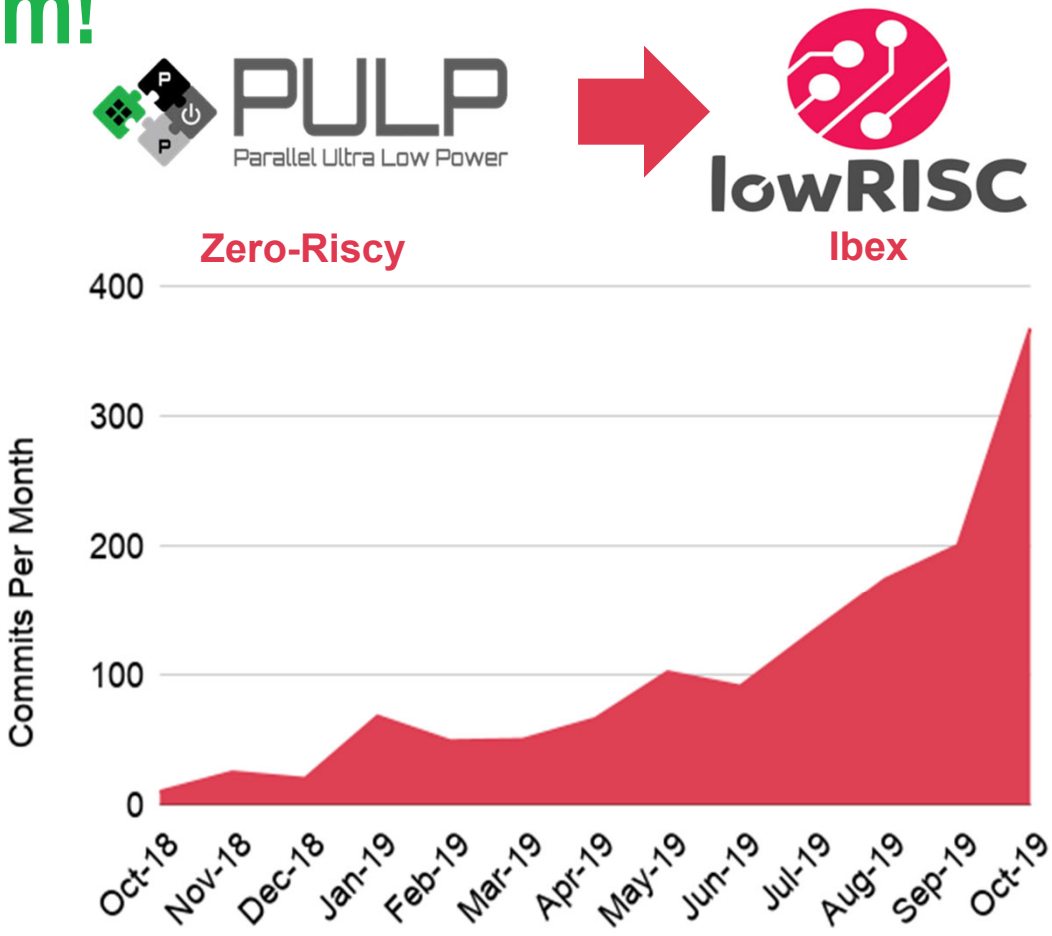
# Feel the momentum!

Ibex RISC-V core, flash interface, communications ports, cryptography accelerators, and more.

**35+** Contributors

**1300+** Contributions

**470** GitHub Issues



# Academic open source → Industrial open source

OPENHW GROUP — PROVEN PROCESSOR IP

**Rick O'Connor (OpenHW CEO, former RISC-V foundation director)**

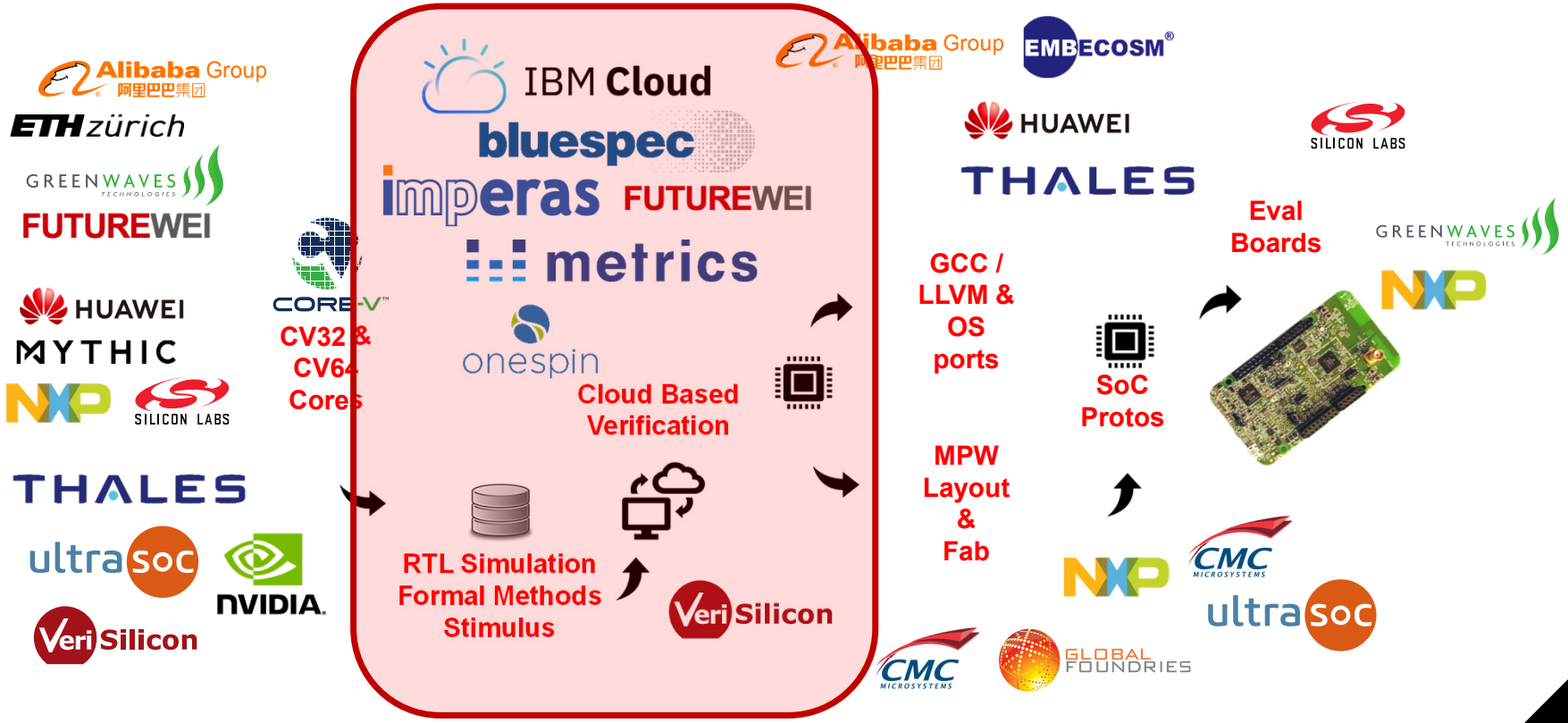
- **OpenHW Group** is a not-for-profit, global organization (EU,NA,Asia) where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the **Core-V** family
- **OpenHW Group** provides an infrastructure for hosting high quality open-source HW developments in line with industry best practices.

PULP — Parallel Ultra Low Power

**RI5CY, ARIANE**

CORE-V™

# OpenHW Group Ecosystem




**Verification is Key!**

# The role of public EU funding

- **Facilitate OSCHW (Europractice++)**
  - Tech. access and MPW cost (including substrate, packaging)
  - EU-supported SoC harnesses (closed-source IP “bulk licensing”)
  - Access to advanced EDA Tools + Expertise (e.g. licensing, cockpits, mixed flows)
  - Design implementation support + Expertise (e.g. Backend, Packaging…)
- **Nurture & Support the ecosystem**
  - OpenHWGroup.EU organization around RISC-V open ISA
  - Develop commercial “physical-IP” ecosystem with easy access for EU companies
  - Open-source EU EDA tooling: research & companies & business model
  - Education-centric initiatives (+Training)

**Big risk: Fragmentation!!**

# PULP

## Parallel Ultra Low Power

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