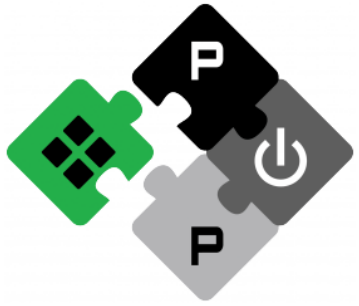

PULP PLATFORM

Open Source Hardware, the way it should be!

Open-Source Hardware for Europe

Luca Benini <luca.Benini@unibo.it, lbenini@iis.ee.ethz.ch>

http://pulp-platform.org

@pulp_platform

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Open Source Hardware

Hardware whose design is made publicly available so that anyone can study, modify, distribute, make, and sell the design or hardware based on that design

(*source: Open Source Hardware (OSHW) Statement of Principles 1.0*)

Very wide definition – includes PCBs and makers' stuff

I will focus on Open Souce Computing Hardware (OSCHW)

OSCHW Needs an Open Source ISA

A modern, open, free ISA, extensible *by construction*
Endorsed and Supported by 600+ Members
But… an open ISA is not Open HW (it's a prerequisite!)

Risc-V international moved to Zürich, CH
for international neutrality, 1/3 of members from EU

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RISC-V is a game changer

OS SW listed (not complete)

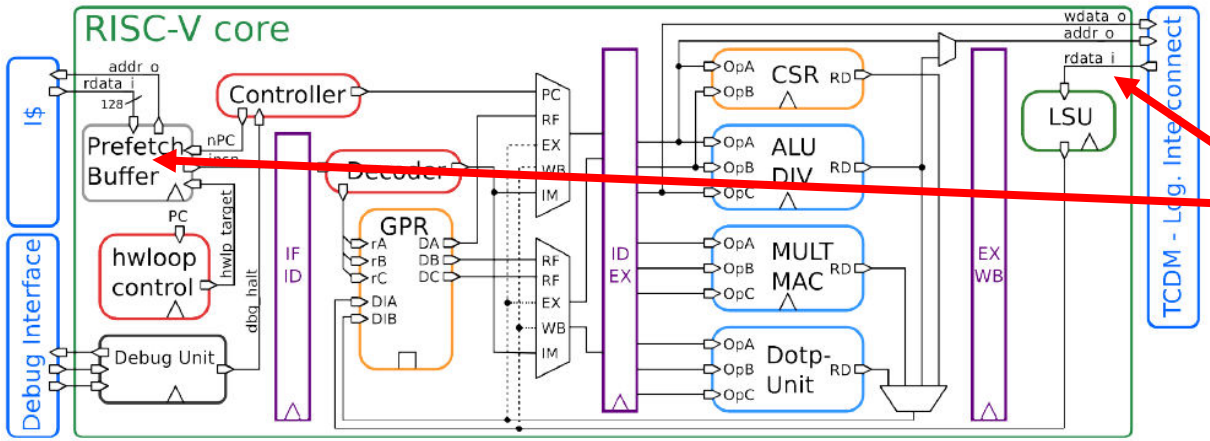
It's the Software, stupid!

- Toolchains → GCC, LLVM
- System tools → Emulators: QEMU, TinyEMU, Spike, Renode
  Bootloaders: Coreboot, U-boot, BBL, OpenSBI
  BINUTILS, GDB, OpenOCD, Glibc, Musl, Newlib
- Language Runtimes → C, C++, Fortran, GO, Rust, Java, Ocaml,
- Operating Systems → Linux: Fedora, OpenSUSE, Gentoo, OpenEmbedded/Yocto, Buildroot, OpenWRT, FreeBSD
  FreeRTOS, Zephyr, RTEMS, Xv6, HelenOS

https://github.com/riscv/riscv-software-list

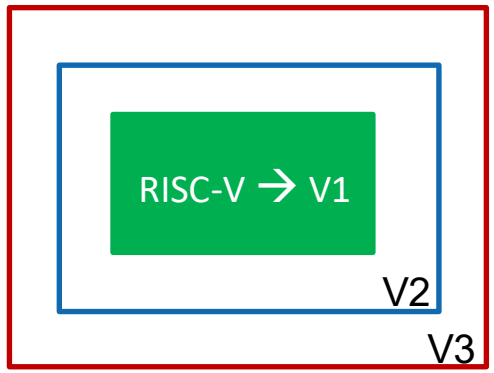
Open HW Core → ISA & Microarchitecture tuning

RI5CY – An Open MCU-class RISC-V Core for EE-AI
3-cycle ALU-OP, 4-cyle MEM-OP→IPC loss: LD-use, Branch



RISC-V®
ISA is extensible *by construction*

I, D mem IF tuned for low latency & time borrowing



V1 Baseline RISC-V RV32IMC (not good for ML)

V2 HW loops. Post modified Load/Store, MAC

V3 SIMD 2/4 + DotProduct + Shuffling.Bit manipulation, Lightweight fixed point

XPULP extensions: 25 kGE → 40 kGE (1.6x) but 9x ML perf!

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PULP: not only cores – many IPs for a Platform

RISC-V Cores

RI5CY	Ibex	Snitch	Ariane + Ara
32b	32b	32b	64b

Peripherals

JTAG	SPI
UART	I2S
DMA	GPIO

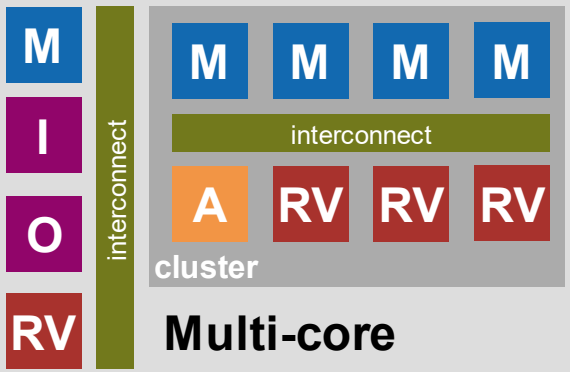
Interconnect

- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

Platforms

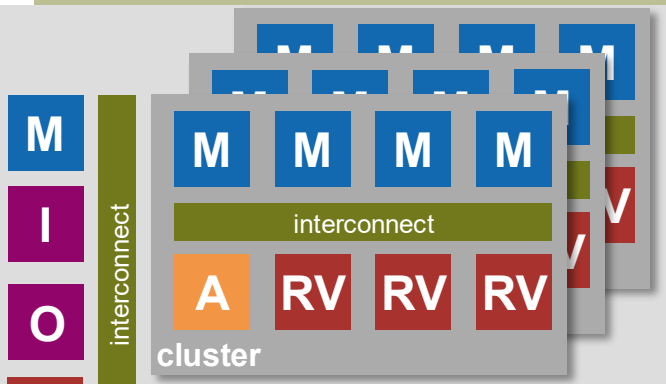
Single Core

- PULPino
- PULPissimo



Multi-core

- Open-PULP
- PULP-PM



Multi-cluster

- Hero
- Manticore

IOT → HPC

Accelerators

HWCE (convolution)	Neurostream (ML)	HWCrypt (crypto)	PULPO (1st ord. opt)

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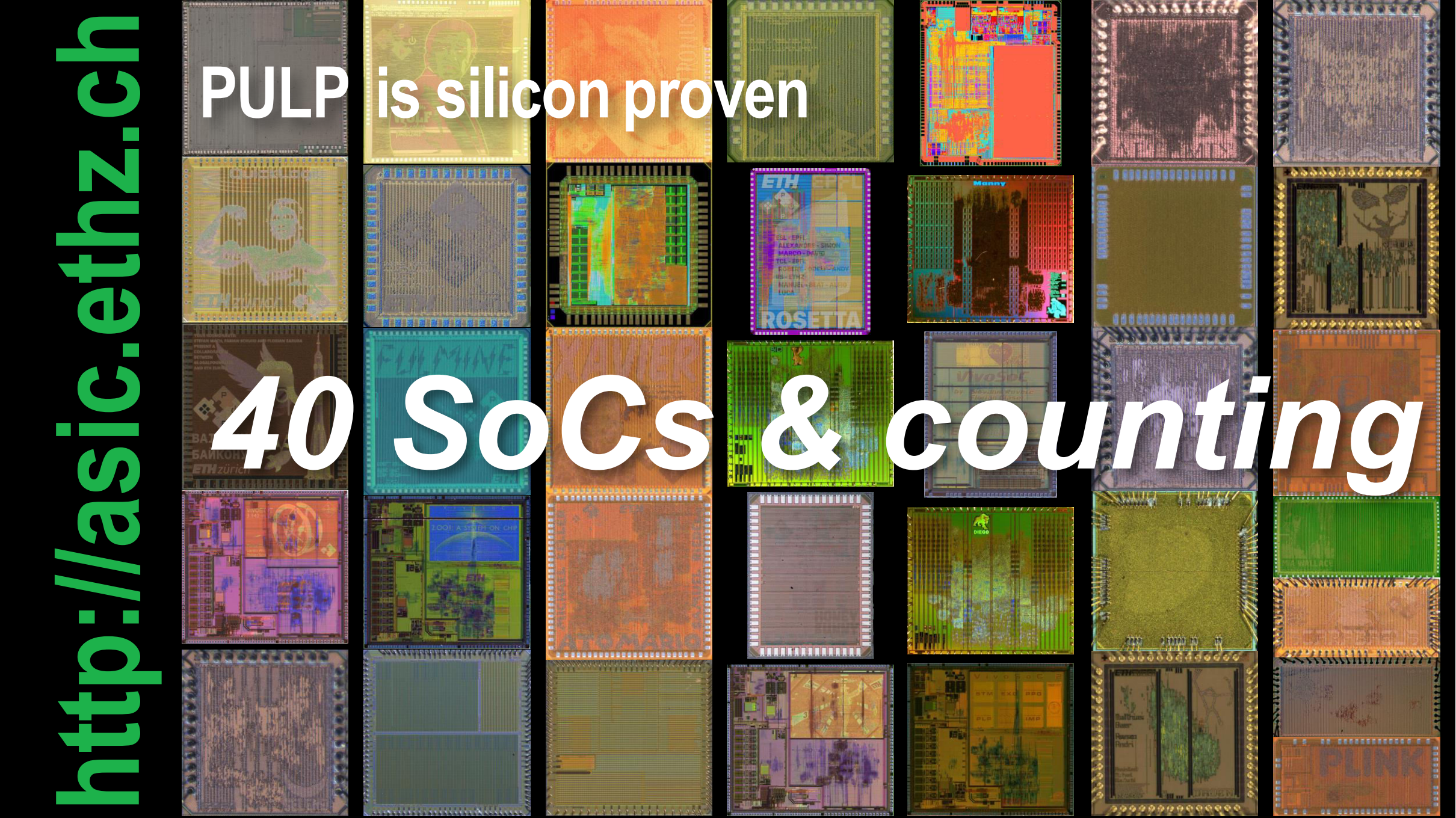
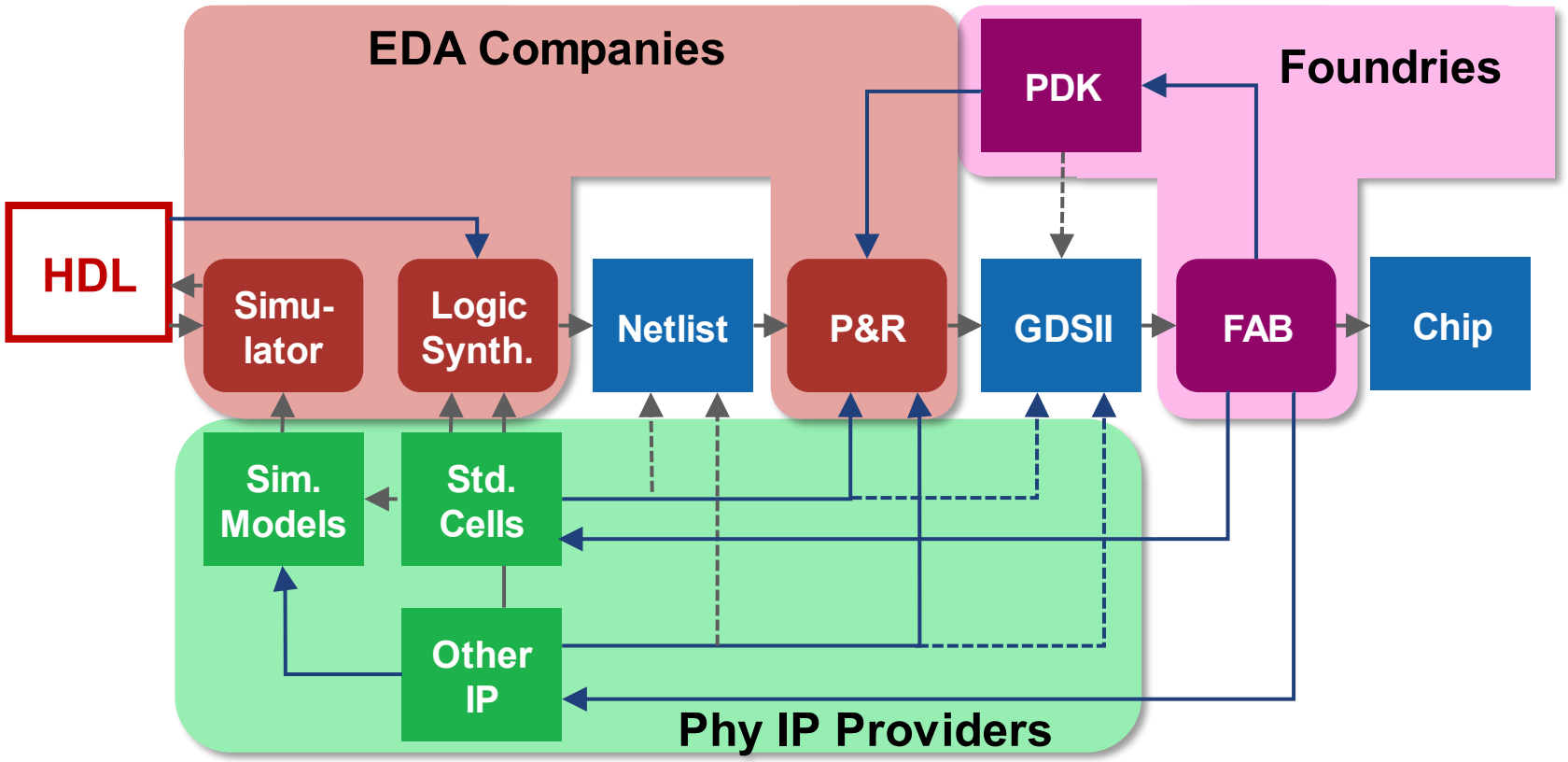

http://asic.ethz.ch
PULP is silicon proven
40 SoCs & counting

Nice, but what exactly is “open” in OSCHW?

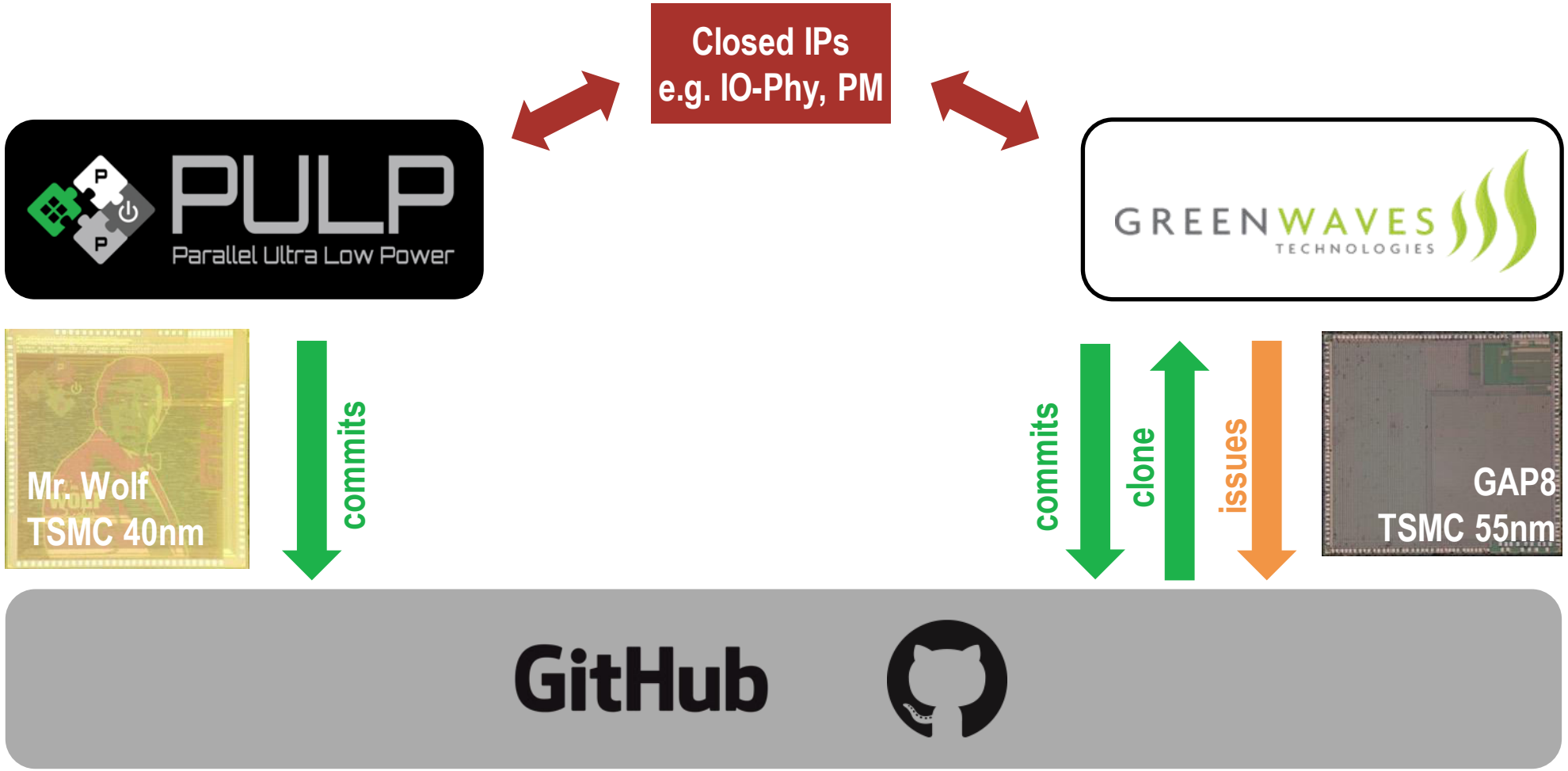
- Only the first stage of the silicon production pipeline
  → **RTL source code** (***permissive****, e.g. Apache is key for industrial adoption)
- Later stages contain closed IP of various actors → not open source by default



Cadence academic tools license forbids ***permissive*** open sourcing of designs made with CDNS tools unless a ***reciprocal**** license is used

“See: https://cern-ohl.web.cern.ch/ (CERN-OHL-S, -W, -P)

Open source collaboration scheme explained



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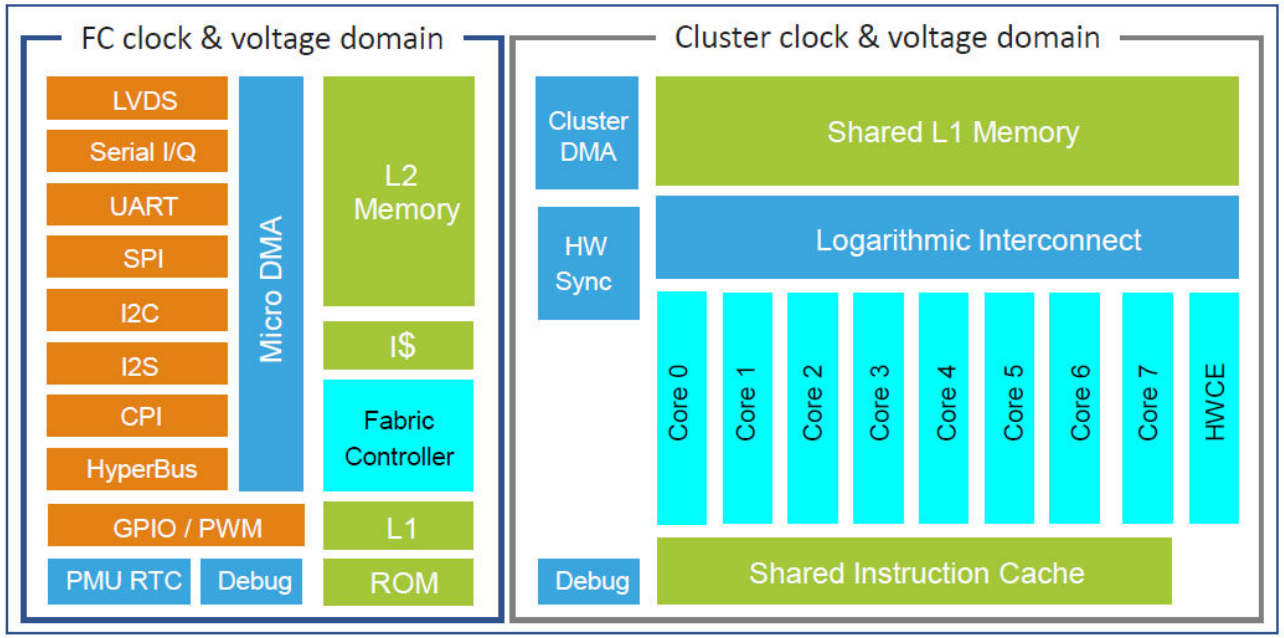
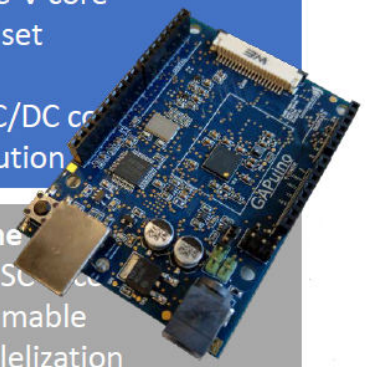
Successful product development: GWT's GAP8

Two independent clock and voltage domains, from 0-133MHz/1V up to 0-250MHz/1.2V



MCU Function
- Extended RISC-V core
- Extensive I/O set
- Micro DMA
- Embedded DC/DC c
- Secured execution



Computation engine
- 8 extended RISC
- Fully programmable
- Efficient parallelization
- Shared instruction cache
- Multi channel DMA
- HW synchronization
- HW convolution Engine

What	Freq MHz	Exec Time ms	Cycles	Power mW
40nm Dual Issue MCU	216	99.1	21 400 000	60
GAP8 @1.0V	15.4 (175)	99.1	1 500 000	3.7
GAP8 @1.2V	17.5	8.7	1 500 000	70
GAP8 @1.0V w HWCE	4.7	99.1	460 000	0.8

11 X

16 X

GREENWAVES TECHNOLOGIES

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Integrating Accelerators into PULP – The big picture

RISC-V Cores

RI5CY	Ibex	Snitch	Ariane + Ara
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DMA	GPIO

Interconnect

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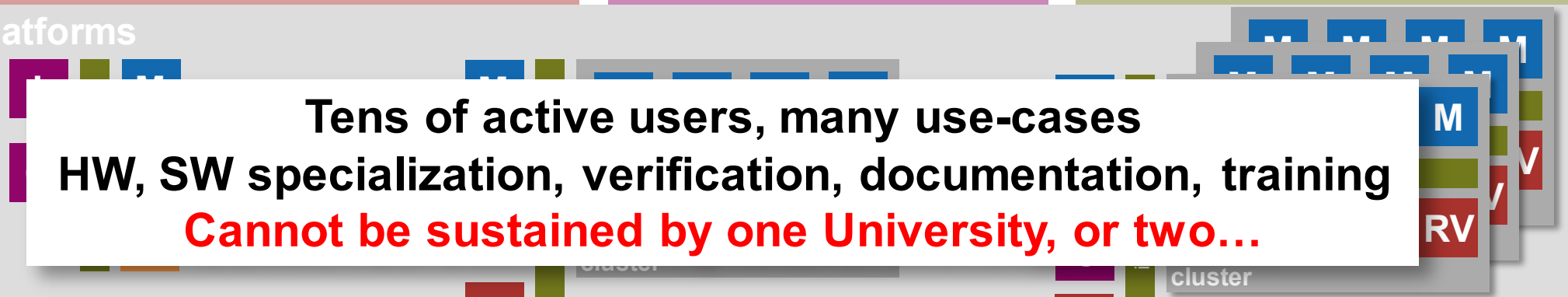
- APB – Peripheral Bus
- AXI4 – Interconnect

Platforms

Tens of active users, many use-cases
HW, SW specialization, verification, documentation, training
Cannot be sustained by one University, or two…



Single Core
- PULPino
- PULPissimo

Multi-core
- Open-PULP
- PULP-PM

Multi-cluster
- Hero
- MANTICORE

IOT → HPC

Accelerators

HWCE (convolution)	Neurostream (ML)	HWCrypt (crypto)	PULPO (1st ord. opt)

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Academic open source → Industrial open source

OPENHW GROUP™ PROVEN PROCESSOR IP

Rick O'Connor (OpenHW CEO, former RISC-V foundation director)

- **OpenHW Group** is a not-for-profit, global organization (EU,NA,Asia) where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the **Core-V** family
- **OpenHW Group** provides an infrastructure for hosting high quality open-source HW developments in line with industry best practices.

PULP Parallel Ultra Low Power

RI5CY, ARIANE

CORE-V™

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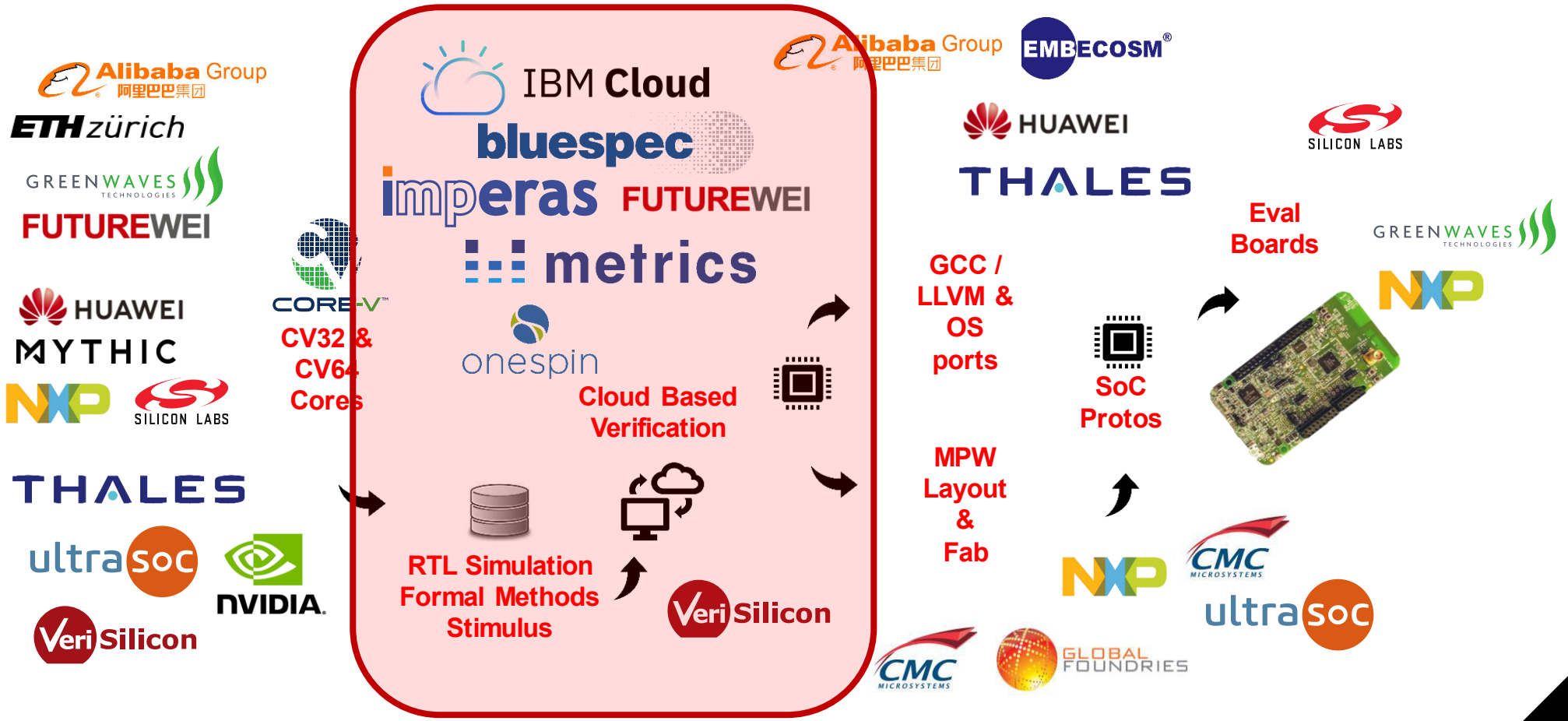
OpenHW Group Ecosystem



Verification is Key!

A vertical, application-focused open approach

- OpenTitan is **the first open source** silicon project building a transparent, high-quality reference design for silicon root of trust (RoT) chips.
- Founding Partners

lowRISC ETH zürich G+D Mobile Security

Google nuvoTon Western Digital.

SEAGATE

ETH zürich

Feel the momentum!

Ibex RISC-V core, flash interface, communications ports, cryptography accelerators, and more.

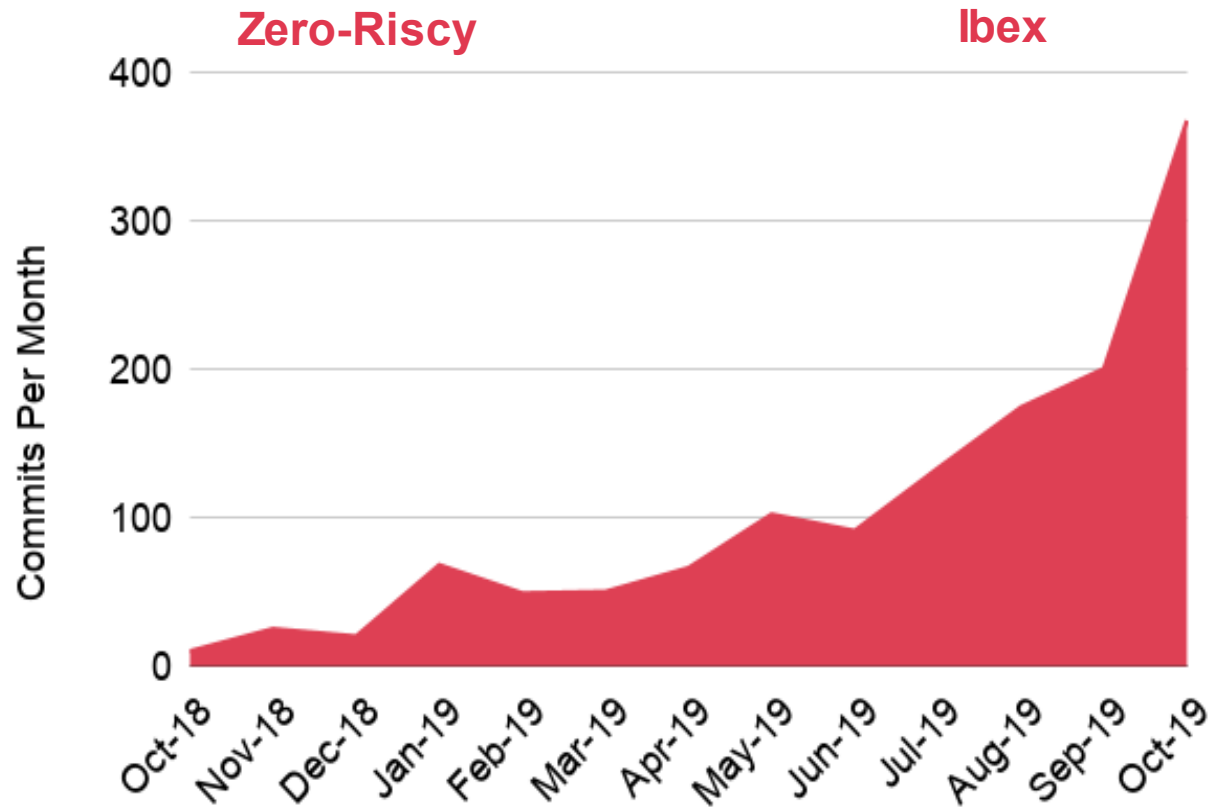
Vibrant repository

35+ Contributors

1300+ Contributions

470 GitHub Issues

PULP Parallel Ultra Low Power → lowRISC



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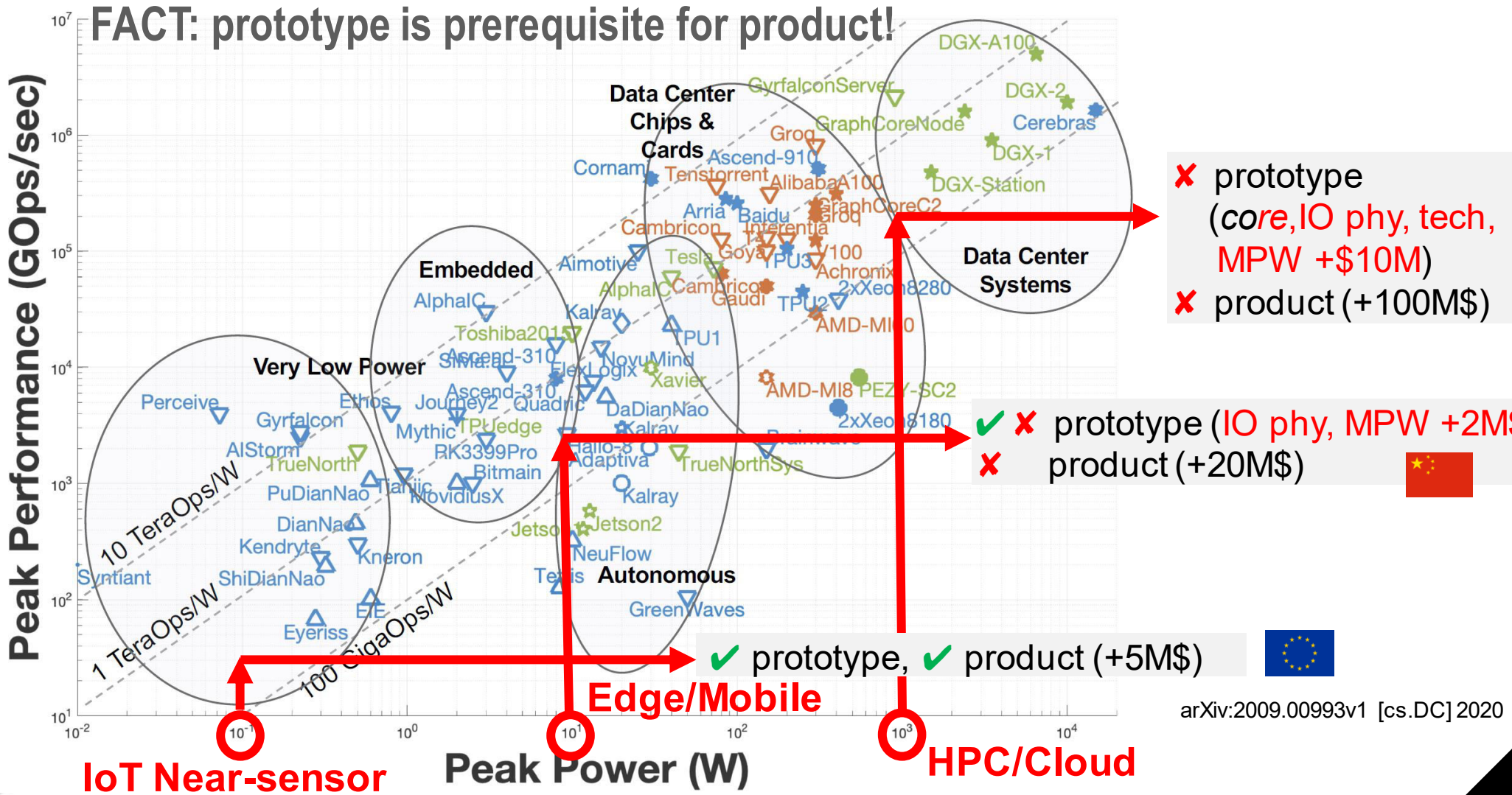
OSCHW prototype & product feasibility?



arXiv:2009.00993v1 [cs.DC] 2020

What about End-to-End Open HW (pdk, tools)?

Open Source
Shuttle Program

Google
+efabless.com

START HERE

Open source process design kit for usage with SkyWater Foundry 130nm tech.
https://github.com/google/skywater-pdk

ASIC EDA flows
http://opencircuitdesign.com/qflow/

FOSS 130nm Production PDK

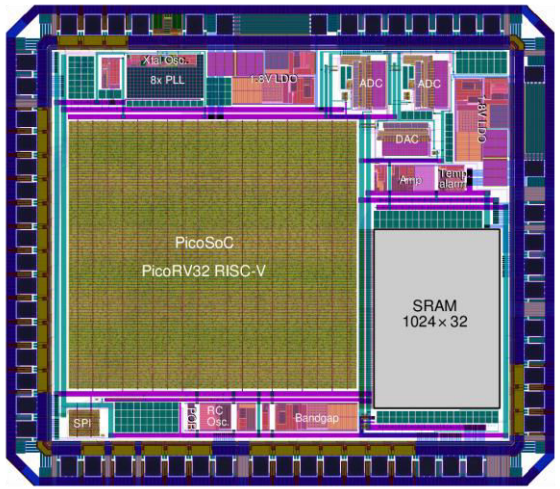
We are excited to collaborate with Google to create engagement and accelerate design on the FOSS 130nm Production PDK.

Efabless will make designs for this PDK simple and affordable by integrating resources on our cloud-based design platform, including:

- An open-source-based end-to-end ASIC design flow, including OpenRoad, Electric, Magic, and others
- The open-source striVe family of full ASIC reference designs
- A marketplace for monetizing your IP or designs

Additionally - Efabless is managing an **Open Source Shuttle Program** sponsored by Google.

The first shuttle is targeted for November 2020 and will provide 40 project slots, free of charge to any fully open-source design.



Raven 130nm mixed-signal SoC

The role of public EU funding

- **Facilitate prototyping of OSCHW (Europractice++)**
  - Tech. access and MPW cost (including substrate, packaging)
  - Enablement (e.g. PLL) + IO/PHY (e.g. HBM) IPs cost
  - Access to advanced EDA Tools + Expertise (e.g. advanced EDA cockpits)
  - Design implementation support + Expertise (e.g. Backend, Packaging…)
- **Nurture & Support the ecosystem**
  - EU Supported OpenHWGroup around Risc-V
  - Develop commercial EU IP ecosystem with facilitated access for EU companies
  - EU EDA tooling: research and companies
  - Education-centric initiatives (+Training)

Closing thoughts… the open HW revolution

For science … fundamental "research infrastructure"

- Community building: sharing of ideas, artefacts
- Fantastic tool for dissemination (more citations ☺)!
- Reduce "getting up to speed" overhead for partners
- Enables fair and well controlled benchmarking

For Business … it is truly disruptive

- Reduces the NRE cost for silicon design
- Faster innovation path for startups
- New business models (for profit and non-for profit)
- Helps exchange of information across NDA walls
- Great for Marketing & Training

For society …long term sustained benefits

- More innovation, growth, jobs
- Personalized silicon vision "Moore-for-all"
- More Secure, safe, auditable HW

DARPA

Posh Open Source Hardware (*POSH*):
An open source System on Chip (SoC) design and verification eco-system that enables cost effective design of ultra-complex SoCs

USA's
electronics resurgence initiative

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PULP

Parallel Ultra Low Power

Luca Benini, Davide Rossi, Andrea Borghesi, Michele Magno, Simone Benatti, Francesco Conti, Francesco Beneventi, Daniele Palossi, Giuseppe Tagliavini, Antonio Pullini, Germain Haugou, Lukas Cavigelli, Manuele Rusci, Florian Glaser, Renzo Andri, Fabio Montagna, Bjoern Forsberg, Pasquale Davide Schiavone, Alfio Di Mauro, Victor Javier Kartsch Morinigo, Tommaso Polonelli, Fabian Schuiki, Stefan Mach, Andreas Kurth, Florian Zaruba, Manuel Eggimann, Philipp Mayer, Marco Guermandi, Xiaying Wang, Michael Hersche, Robert Balas, Antonio Mastrandrea, Matheus Cavalcante, Angelo Garofalo, Alessio Burrello, Gianna Paulin, Georg Rutishauser, Andrea Cossettini, Luca Bertaccini, Maxim Mattheeuws, Samuel Riedel, Sergei Vostrikov, Vlad Niculescu, Frank K. Gurkaynak,
and many more that we forgot to mention

http://pulp-platform.org @pulp_platform